

MODEL NAME : VAUB0

PCB NO : LA-9941P
DAA0006W000

BOM P/N : TBD

Dell/Compal Confidential

Schematic Document

Phantom (Shark Bay)

Hasweill (BGA) + Lynx Point

DISCRETE VGA N14P (optimus) --- Testarossa
DISCRETE VGA N15P (optimus) --- Testarossa-P

2013-01-02

Rev: 0.1 (X00)

@ : Nopop Component

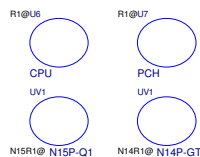
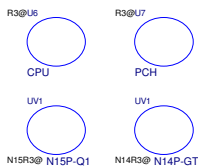
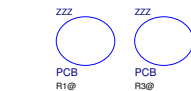
CONN@ : Connector Component

TPM@ : TPM function

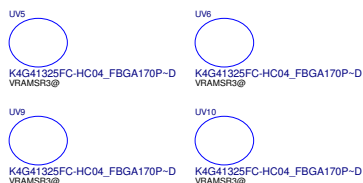
DSP@ : DSP function

N14@ : DGPU N14P-GT

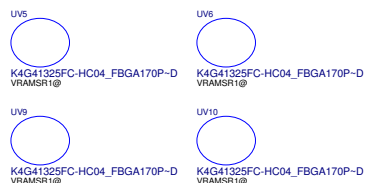
N15@ : DGPU N15P-Q1



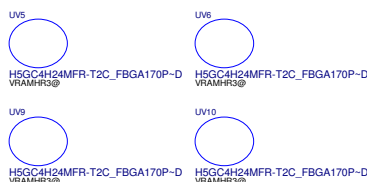
Samsung 2G



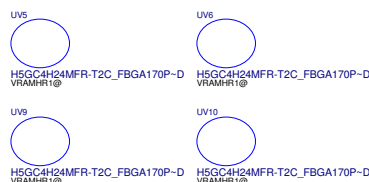
Samsung 2G



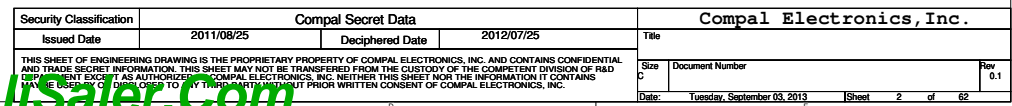
Hynix 2G



Hynix 2G

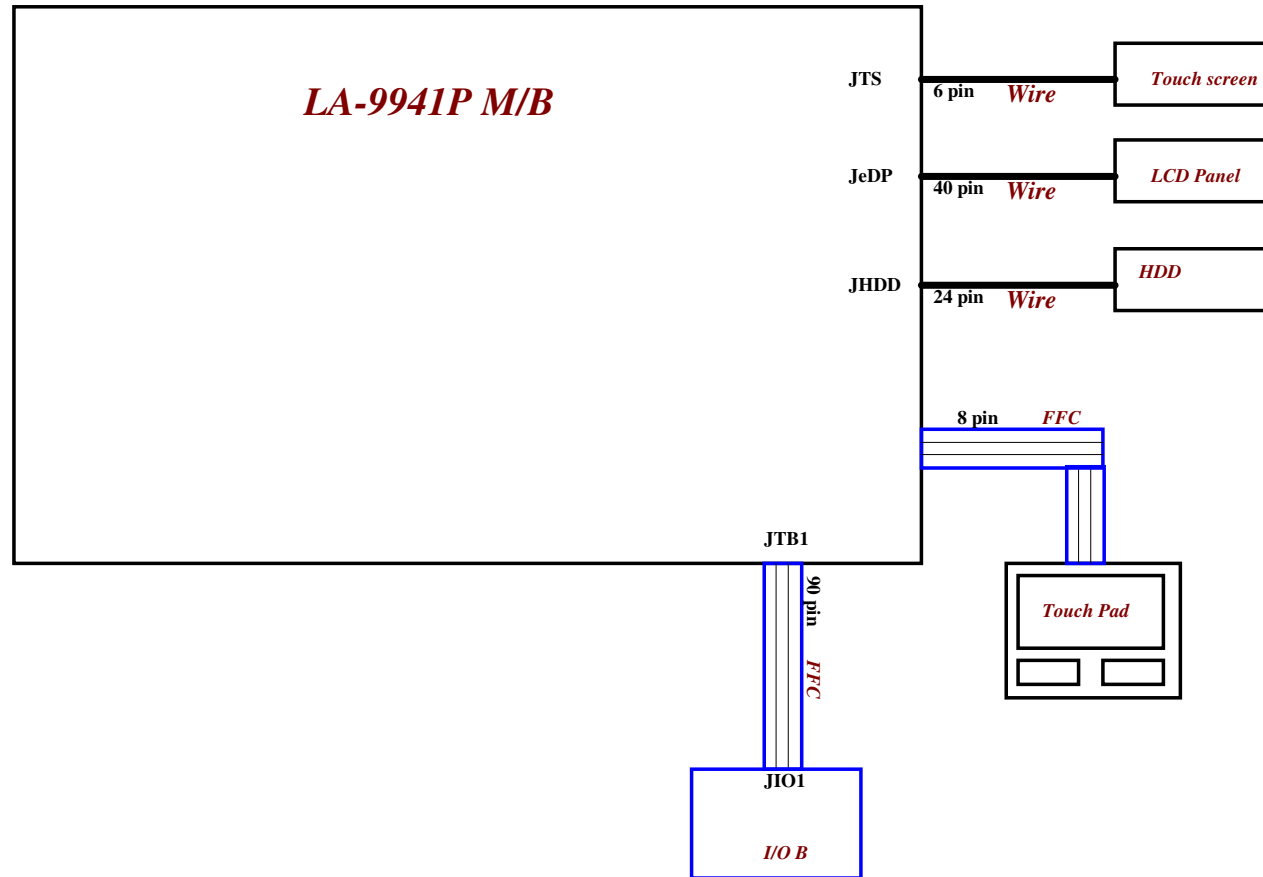


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Project Code : VAUB0

File Name : LA-9941P



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Board ID	PCB Revision	Board ID	PCB Revision
0	DIS 0.1	0	DIS 0.1
1	DIS 0.2	1	DIS 0.2
2	DIS 0.3	2	DIS 0.3
3	DIS 0.4	3	DIS 0.4
4	DIS 0.5	4	DIS 0.5
5	DIS 1.0	5	DIS 1.0
6	DIS-P 0.2	6	DIS-P 0.2
7	DIS-P 0.3	7	DIS-P 0.3
8	DIS-P 0.4	8	DIS-P 0.4
9	DIS-P 1.0	9	DIS-P 1.0
10	UMA 0.2	10	UMA 0.2
11	UMA 0.3	11	UMA 0.3
12	UMA 0.4	12	UMA 0.4
13	UMA 1.0	13	UMA 1.0
14		14	
15		15	
16		16	
17		17	
18		18	
19		19	

USB PORT#	DESTINATION
0	USB Conn 1 (Power share)
1	USB Conn 3 (Power share)
2	USB Conn 2 (Power share)
3	USB Conn 4 (Power share)
4	JMINI1 (WLAN)
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA
13	None

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

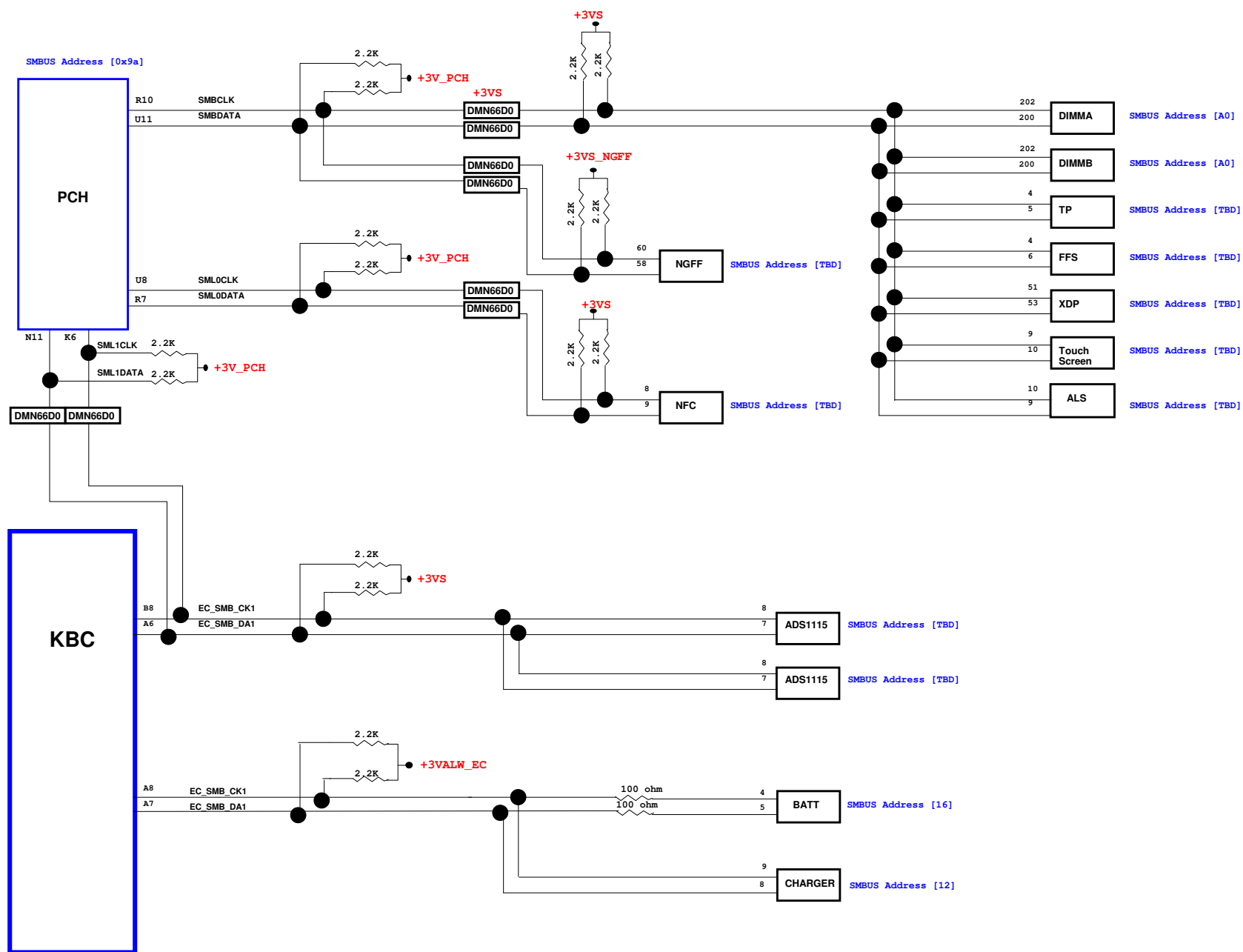
USB3	DESTINATION
1	USB Conn 1 (Power share)
2	USB Conn 3 (Power share)
3	USB Conn 2 (Power share)
4	USB Conn 4 (Power share)

DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
CLKOUT_PCIE1	None	CLKOUTFLEX1	None
CLKOUT_PCIE2	None	CLKOUTFLEX2	None
CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
CLKOUT_PCIE4	CARD READER		
CLKOUT_PCIE5	None		
CLKOUT_PCIE6	None		
CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None		

Symbol Note :

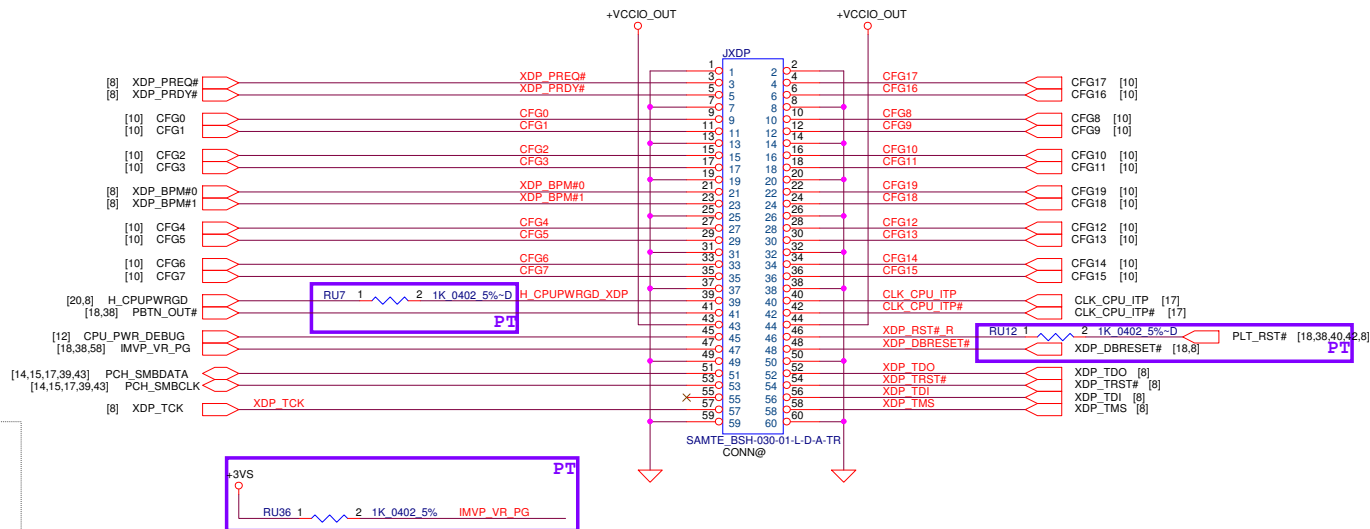
⏏ : means Digital Ground
⏏ : means Analog Ground

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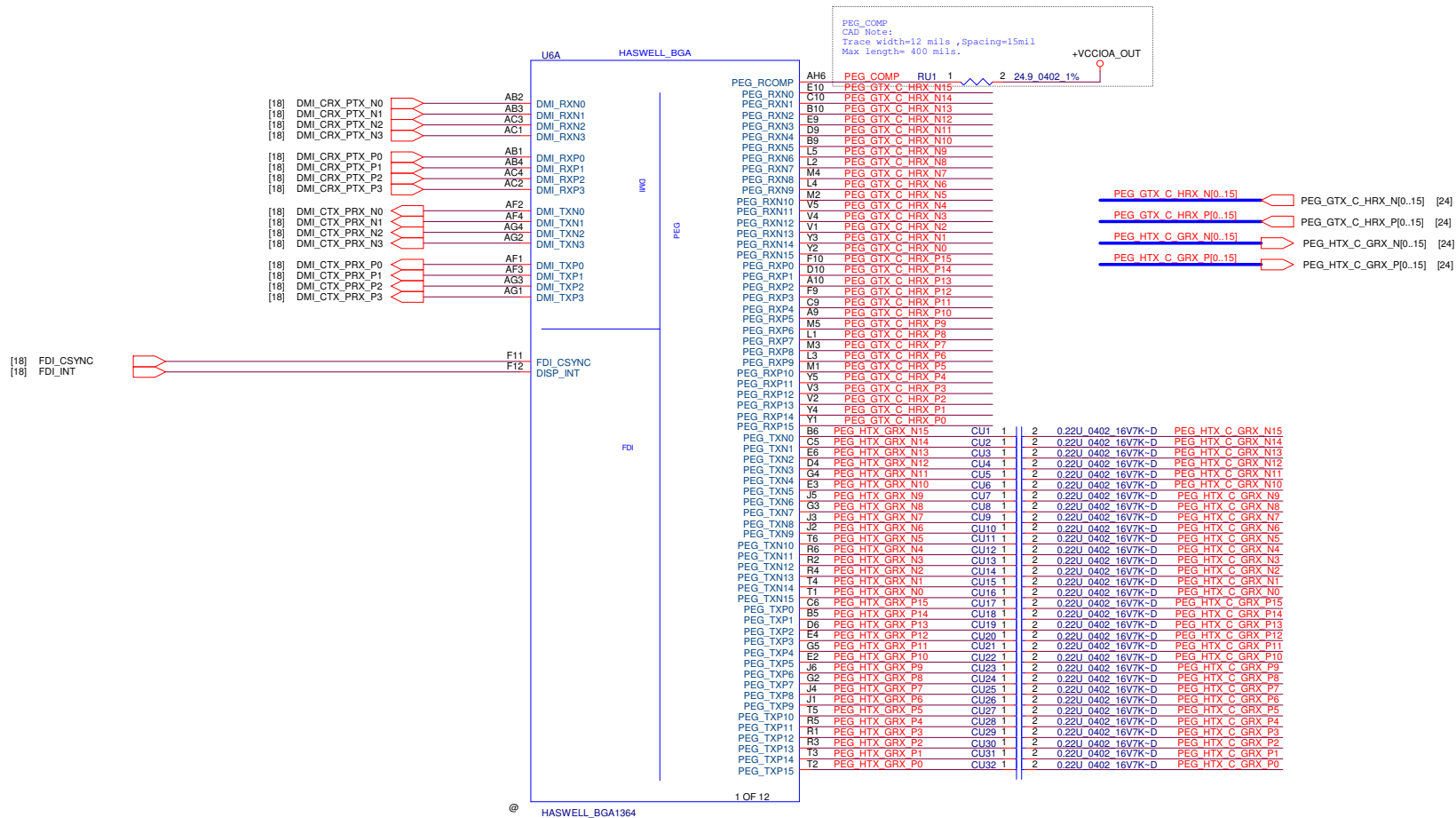


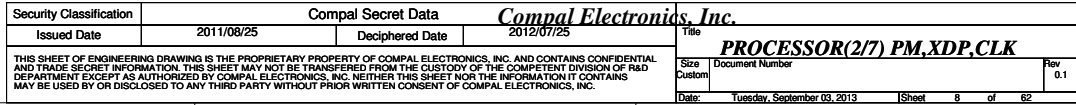
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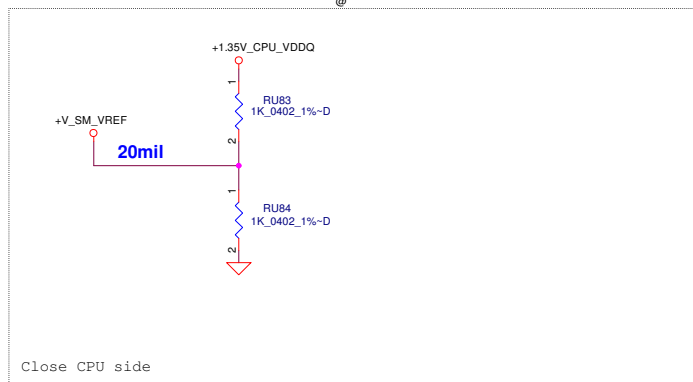
XDP CONN



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				Document Number		Rev	
						0.1	
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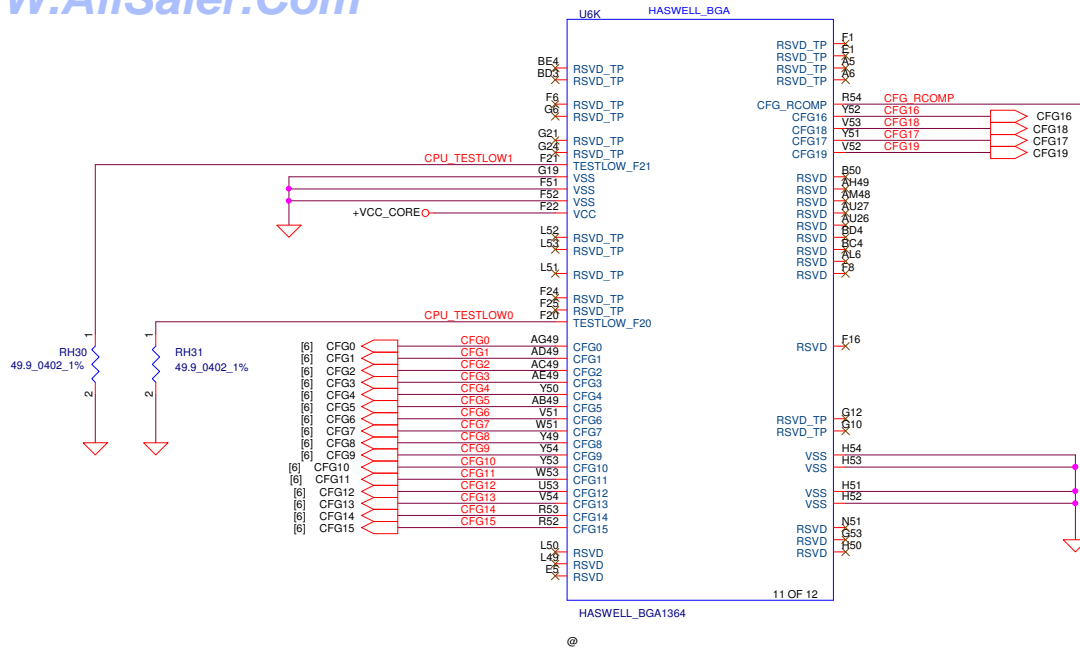






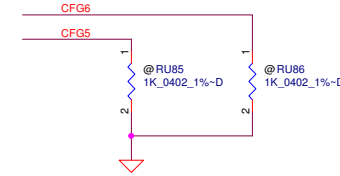
GENERAL Form Size Custom	Document Number	Rev 0.1
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CFG Straps for Processor

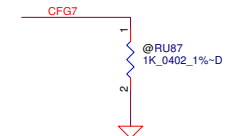


PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

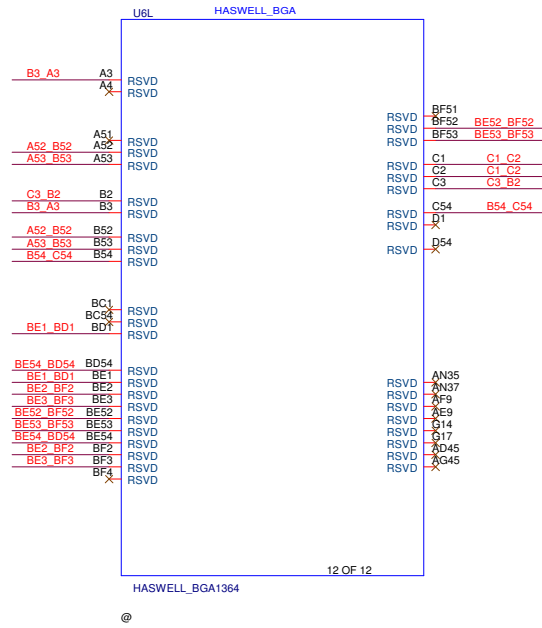
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

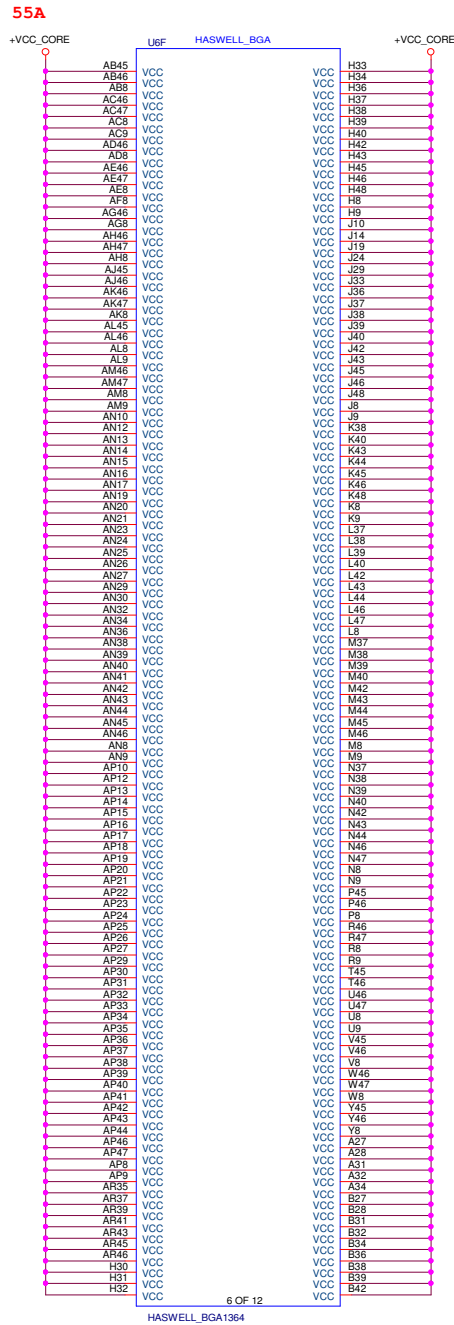


PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

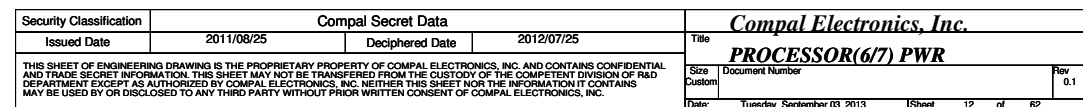


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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U6G HASWELL_BGA		
A11	VSS	AJ48
A15	VSS	AJ51
A19	VSS	AJ54
A22	VSS	AK43
A26	VSS	AK5
A30	VSS	AK50
A33	VSS	AK7
A37	VSS	AK9
A40	VSS	AL1
A44	VSS	AL4
AA1	VSS	AL48
AA2	VSS	AL52
AA3	VSS	AL7
AA4	VSS	AM5
AA48	VSS	AM51
AA5	VSS	AM52
AA7	VSS	AM53
AB5	VSS	AM54
AB51	VSS	AM7
AB52	VSS	AN1
AB53	VSS	AN2
AB54	VSS	AN3
AB7	VSS	AN4
AB9	VSS	AN48
AC48	VSS	AN5
AC5	VSS	AN50
AC50	VSS	AN7
AC7	VSS	AP51
AD48	VSS	AP54
AD51	VSS	AP7
AD54	VSS	AR12
AD7	VSS	AR14
AD9	VSS	AR16
AE1	VSS	AR18
AE2	VSS	AR20
AE3	VSS	AR24
AE4	VSS	AR26
AE48	VSS	AR48
AE5	VSS	AR5
AE50	VSS	AR50
AE7	VSS	AR7
AF5	VSS	AR8
AF6	VSS	AR9
AF7	VSS	AT1
AG48	VSS	AT10
AG5	VSS	AT12
AG51	VSS	AT15
AG52	VSS	AT16
AG53	VSS	AT18
AG54	VSS	AT20
AG7	VSS	AT22
AG9	VSS	AT25
AH1	VSS	AT26
AH2	VSS	AT29
AH3	VSS	AT33
AH4	VSS	AT35
AH48	VSS	AT37
AH5	VSS	AT39
AH50	VSS	AT4
AH7	VSS	

HASWELL_BGA1364

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U6H HASWELL_BGA		
AT40	VSS	AY50
AT42	VSS	AY9
AT43	VSS	B11
AT45	VSS	B15
AT46	VSS	B19
AT47	VSS	B22
AT49	VSS	B26
AT5	VSS	B30
AT50	VSS	B33
AT51	VSS	B37
AT52	VSS	B40
AT53	VSS	B44
AT54	VSS	B49
AT6	VSS	B8
AT8	VSS	BA13
AT9	VSS	BA19
AU13	VSS	BA22
AU18	VSS	BA25
AU22	VSS	BA29
AU25	VSS	BA33
AU29	VSS	BA37
AU33	VSS	BA4
AU37	VSS	BA42
AU42	VSS	BA5
AU5	VSS	BA50
AU9	VSS	BA51
AV1	VSS	BA52
AV13	VSS	BA53
AV18	VSS	BA9
AV2	VSS	BB10
AV22	VSS	BB11
AV25	VSS	BB12
AV29	VSS	BB14
AV3	VSS	BB15
AV33	VSS	BB16
AV4	VSS	BB17
AV42	VSS	BB18
AV5	VSS	BB20
AV50	VSS	BB23
AV9	VSS	BB25
AW13	VSS	BB28
AW18	VSS	BB32
AW37	VSS	BB33
AW42	VSS	BB37
AW43	VSS	BB38
AW45	VSS	BB39
AW46	VSS	BB41
AW47	VSS	BB42
AW49	VSS	BB43
AW5	VSS	BB44
AW50	VSS	BB46
AW51	VSS	BB47
AW54	VSS	BB48
AW9	VSS	BB49
AY13	VSS	BB5
AY22	VSS	BB6
AY25	VSS	BB7
AY29	VSS	BB9
AY33	VSS	
AY37	VSS	
AY42	VSS	

HASWELL_BGA1364

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U6I HASWELL_BGA		
BC10	VSS	G20
BC12	VSS	G23
BC15	VSS	G25
BC18	VSS	G26
BC22	VSS	G30
BC23	VSS	G33
BC3	VSS	G37
BC30	VSS	G40
BC33	VSS	G44
BC36	VSS	G49
BC38	VSS	G52
BC41	VSS	G54
BC43	VSS	G7
BC46	VSS	G8
BC48	VSS	G9
BC5	VSS	H44
BC50	VSS	H49
BC52	VSS	H7
BC7	VSS	J4
BD10	VSS	J49
BD15	VSS	J51
BD18	VSS	J54
BD36	VSS	J7
BD41	VSS	K1
BD46	VSS	K2
BD5	VSS	K3
BD51	VSS	K4
BE10	VSS	K5
BE15	VSS	K6
BE36	VSS	K7
BE4	VSS	L48
BE46	VSS	L7
BF10	VSS	L9
BF12	VSS	M48
BF15	VSS	M50
BF18	VSS	M52
BF22	VSS	M54
BF26	VSS	M7
BF36	VSS	N48
BF38	VSS	N7
BF39	VSS	P1
BF36	VSS	P2
BF38	VSS	P3
BF41	VSS	P4
BF43	VSS	P48
BF46	VSS	P5
BF48	VSS	P50
BF7	VSS	P52
C11	VSS	P54
C15	VSS	P6
C19	VSS	P7
C22	VSS	P7
C26	VSS	R48
C30	VSS	R7
C33	VSS	T48
C37	VSS	U1
C4	VSS	U2
C40	VSS	U3
C44	VSS	U4
C49	VSS	U48
C52	VSS	U5
C5	VSS	U50
D11	VSS	U52
D15	VSS	U54
D19	VSS	U6
D22	VSS	U7
D26	VSS	V48
D30	VSS	V7
D33	VSS	V8
D37	VSS	W48
D40	VSS	W50
D44	VSS	W52
D49	VSS	W54
D8	VSS	W7
E11	VSS	Y48
E15	VSS	Y7
E16	VSS	Y9
E17	VSS	
E19	VSS	
E20	VSS	AR22
E21	VSS	AB48
E22	VSS	P9
E24	VSS	G18
E25	VSS	A49
E26	VSS	A50
E30	VSS	A8
E33	VSS	B4
E37	VSS	BA1
E40	VSS	BA54
E44	VSS	BB1
E49	VSS	BB54
E51	VSS	BD2
E53	VSS	BD53
E8	VSS	BF49
F2	VSS	BF5
F26	VSS	BF50
F3	VSS	BF6
F30	VSS	C53
F37	VSS	D2
F4	VSS	E54
F40	VSS	F54
F44	VSS	G1
F49	VSS	
F5	VSS	
G11	VSS	
G13	VSS	
G16	VSS	

HASWELL_BGA1364

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VSS_SENSE

CAD Note: RU99 SHOULD BE PLACED CLOSE TO CPU

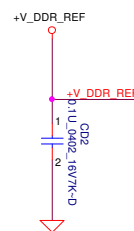
RU99
100_0402_1%-D

VSSSENSE [58]

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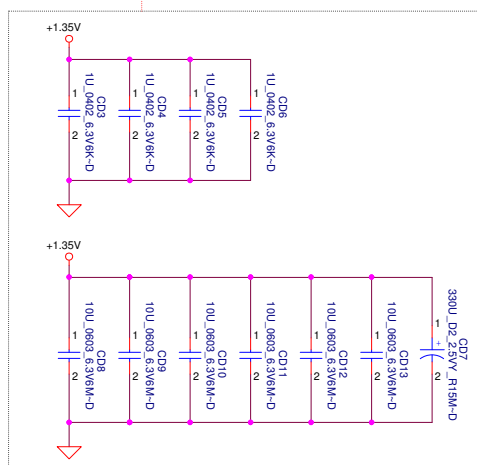
M1

- [9] DDR_A_DQS#[0..7]
- [9] DDR_A_DQS#[0..7]
- [9] DDR_A_D[0..63]
- [9] DDR_A_MA[0..15]

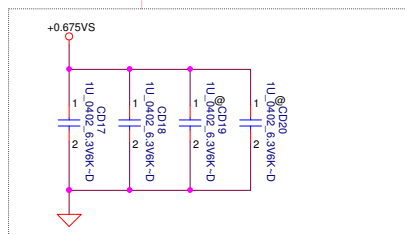


All VREF traces should have 10 mil trace width

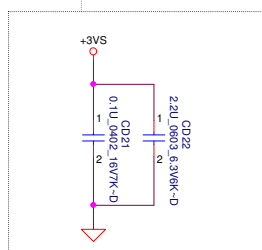
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203, 204



Layout Note:
Place near JDIMM1.199



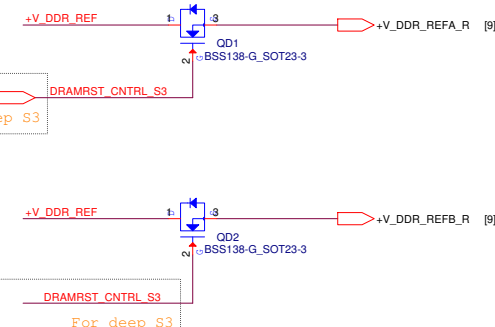
- [9] DDR_CKE0_DIMMA
- [9] DDR_A_BS2
- [9] M_CLK_DDR0
- [9] M_CLK_DDR#0
- [9] DDR_A_BS0
- [9] DDR_A_WE#
- [9] DDR_A_CAS#
- [9] DDR_CS1_DIMMA#
- [9] DDR_CKE1_DIMMA
- [9] DDR_A_MA15
- [9] DDR_A_MA14
- [9] DDR_A_MA11
- [9] DDR_A_MA7
- [9] DDR_A_MA6
- [9] DDR_A_MA4
- [9] DDR_A_MA2
- [9] DDR_A_MA0
- [9] M_CLK_DDR1
- [9] M_CLK_DDR#1
- [9] DDR_A_BS1
- [9] DDR_A_RAS#
- [9] DDR_CS0_DIMMA#
- [9] M_ODT0
- [9] M_ODT1

All VREF traces should have 10 mil trace width

+V_DDR_REF

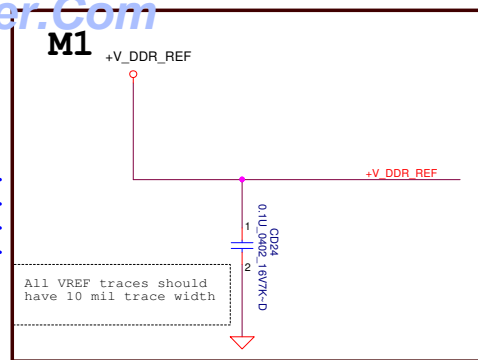
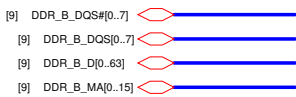


M3

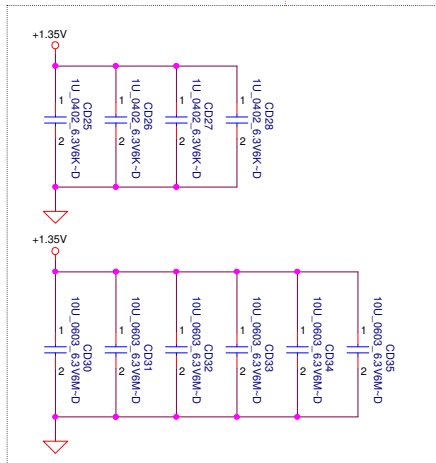
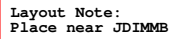


M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

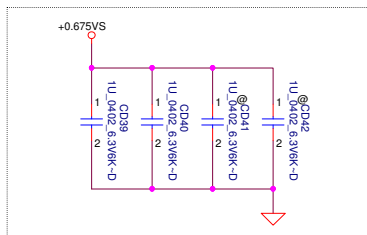
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				Sheet 14 of 62	



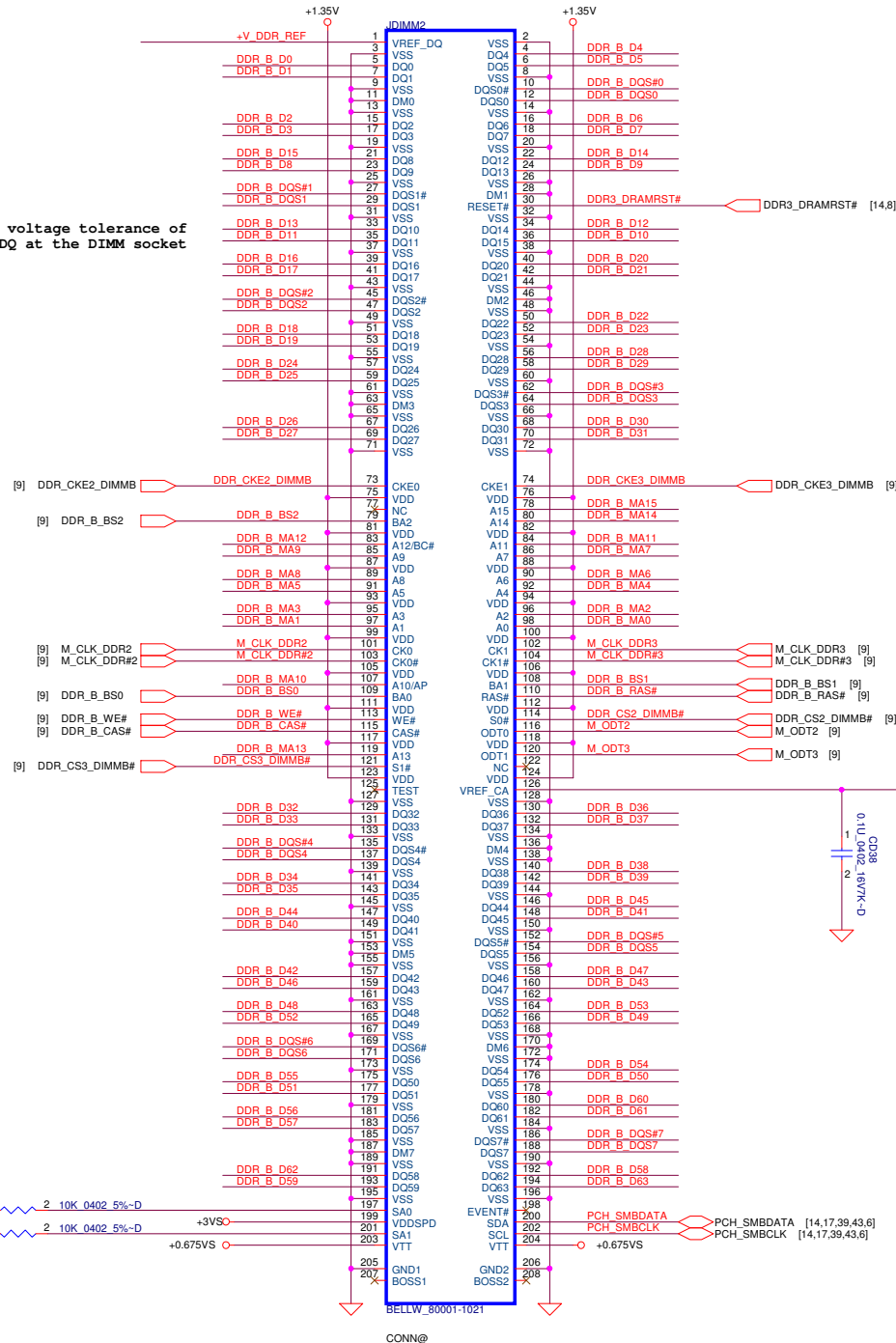
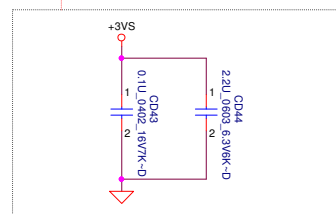
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMMB.203,204

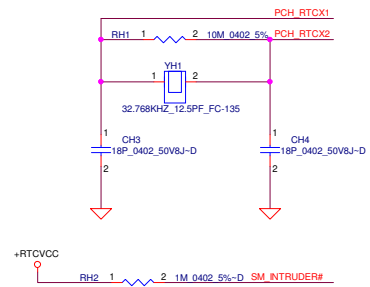


Layout Note:
Place near JDIMMB.199



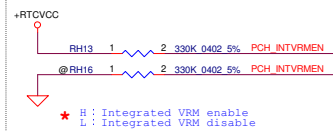
All VREF traces should have 10 mil trace width

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Date: Tuesday, September 03, 2013				Sheet 15 of 62	

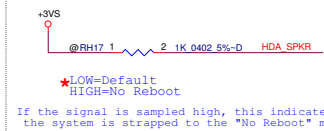


PCH Strap PIN

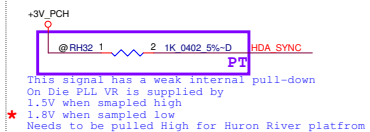
INTVRMEN Integrated 1.05V VRM Enable/Disable



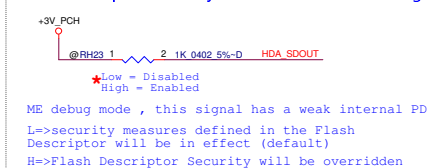
SPKR No Reboot



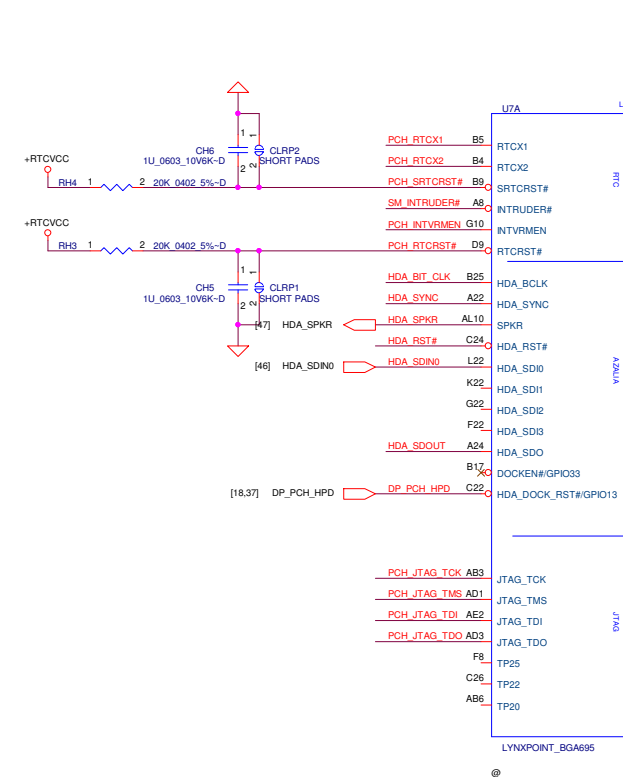
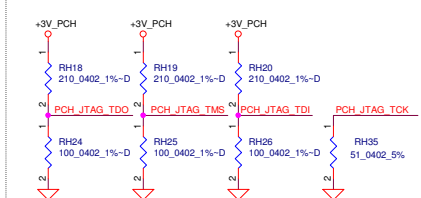
HDA_SYNC On-Die PLL Voltage Regulator Voltage Select



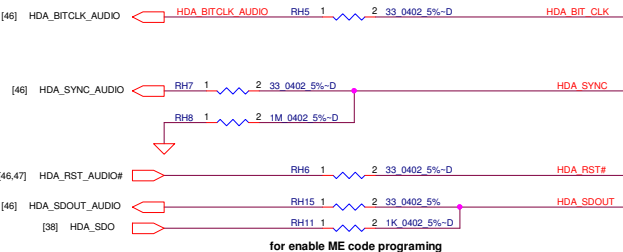
HDA_SDO Flash Descriptor Security Override/Intel ME Debug Mode



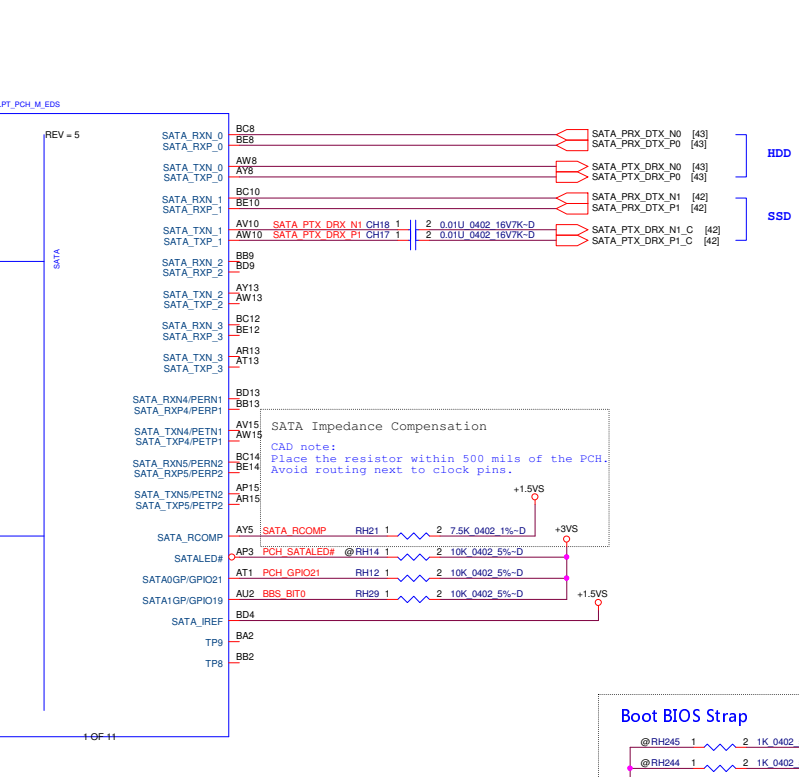
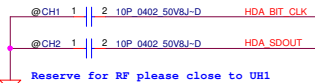
JTAG



HD Audio

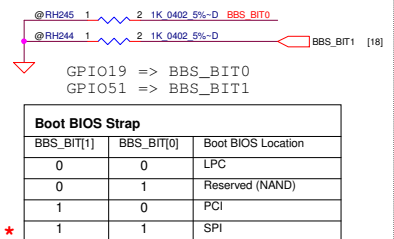


Reserve for EMI



SATA Impedance Compensation
CAD note:
Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

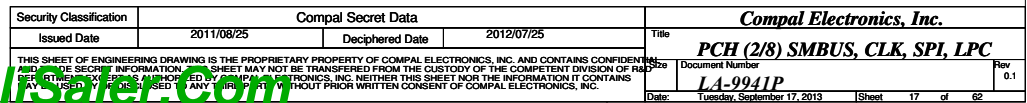
Boot BIOS Strap

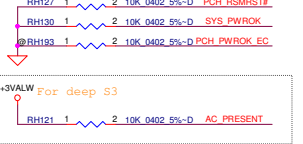
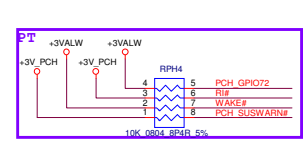
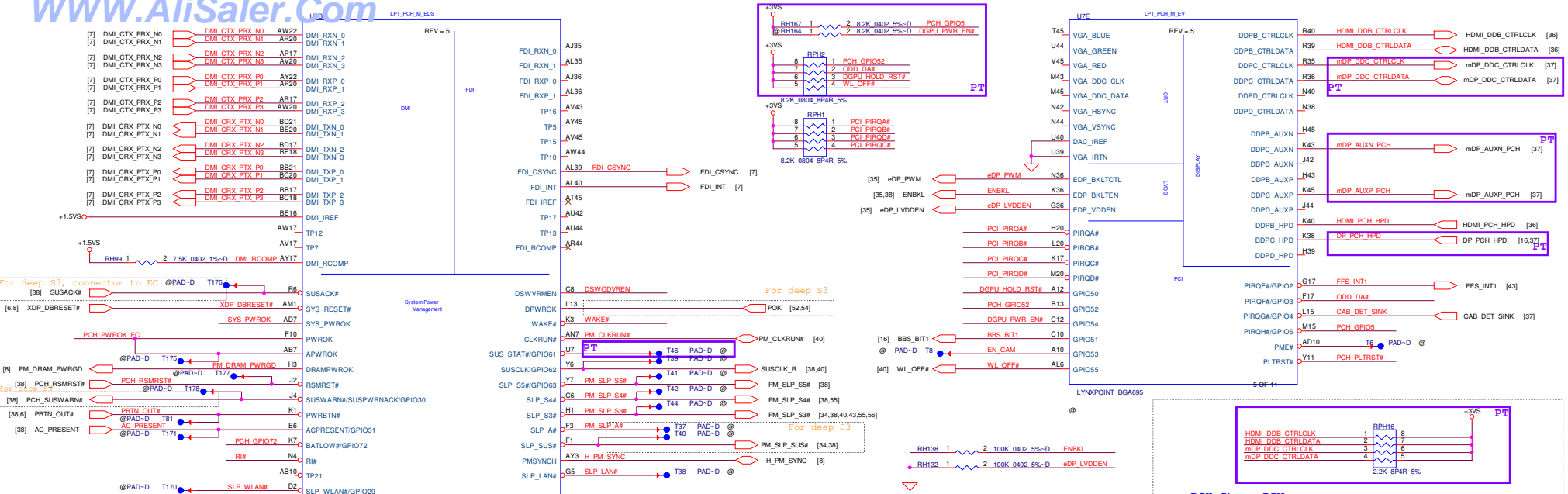


Boot BIOS Strap		
BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

RTC Battery

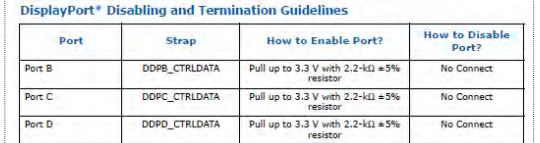
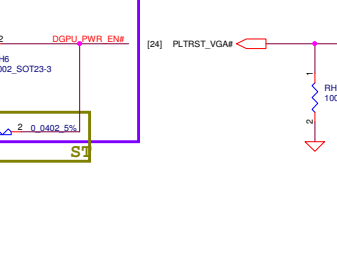
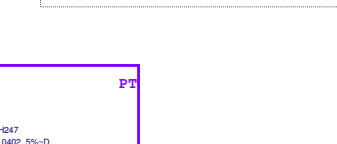
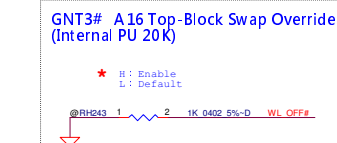
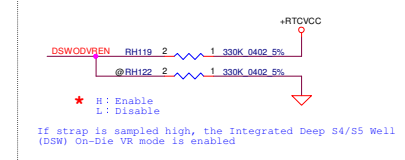




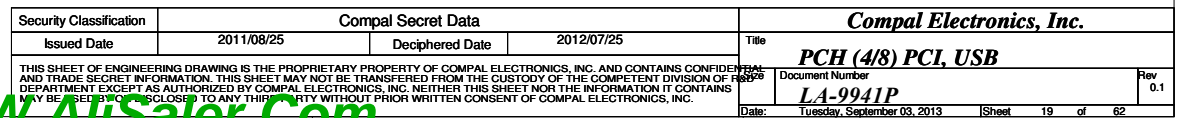


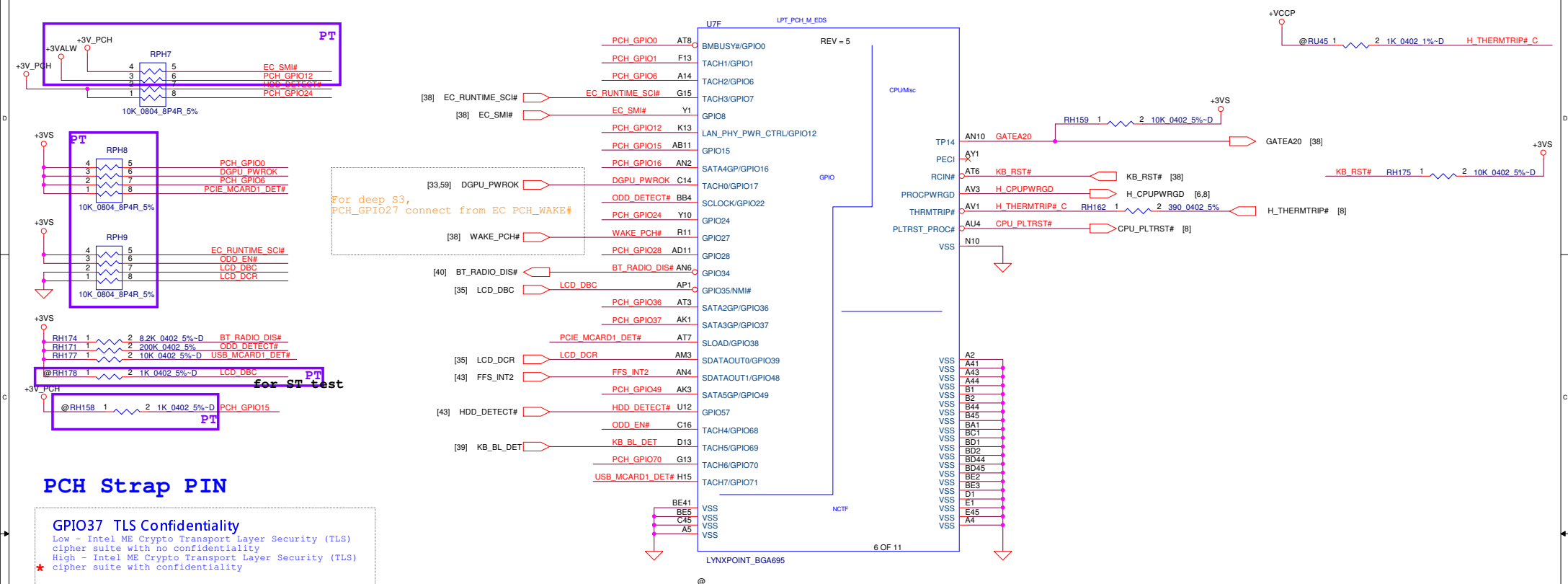
PCH Strap PIN

DSWVRMEN
Deep S4/S5 Well On-Die Voltage Regulator Enable



Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLCLK	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLCLK	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLCLK	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect





PCH Strap PIN

GPIO37 TLS Confidentiality

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
 High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

RH169 1 2 10K 0402 5%-D PCH_GPIO37

GPIO28 On-Die PLL Voltage Regulator

This signal has a weak internal pull up

* H : On-Die voltage regulator enable
 L : On-Die PLL Voltage Regulator disable

@RH165 1 2 1K 0402 5%-D PCH_GPIO28

SATA2GP/GPIO36 Reserved

When Unused as GPIO or SATA*GP -
 Use 8.2K-10K pull-down to ground

@RH194 1 2 10K 0402 5%-D PCH_GPIO36

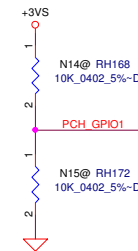
+3VALW

RH173 1 2 10K 0402 5%-D WAKE_PCH#

@RH170 1 2 10K 0402 5%-D

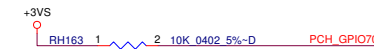


config	GPIO16,GPIO49
* USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

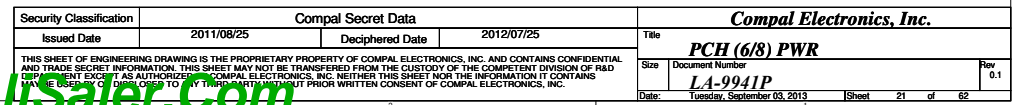


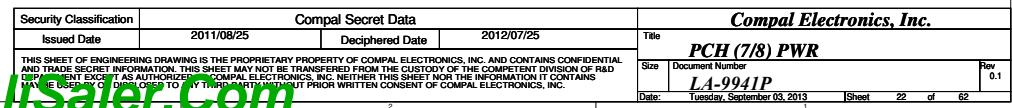
DGPU Board ID Optional

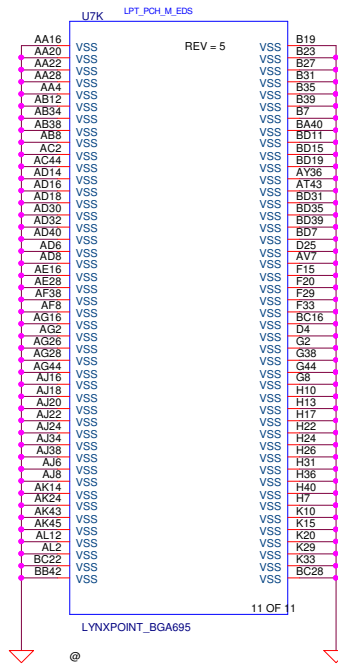
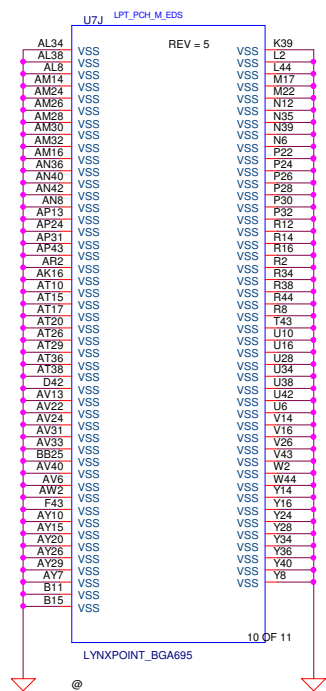
PCH_GPIO1	
N14P	1 = N14P-GT 0 = N15P



PCH_GPIO70	
DIS	1
UMA	0







[7] PEG_HTX_C_GRX_P[0..15] PEG_HTX_C_GRX_P[0..15]
 [7] PEG_HTX_C_GRX_N[0..15] PEG_HTX_C_GRX_N[0..15]
 [7] PEG_GTX_C_HRX_P[0..15] PEG_GTX_C_HRX_P[0..15]
 [7] PEG_GTX_C_HRX_N[0..15] PEG_GTX_C_HRX_N[0..15]

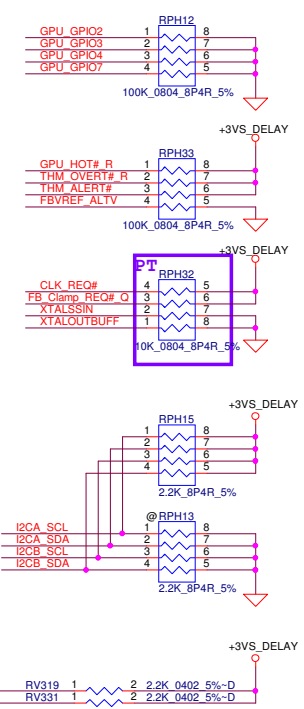
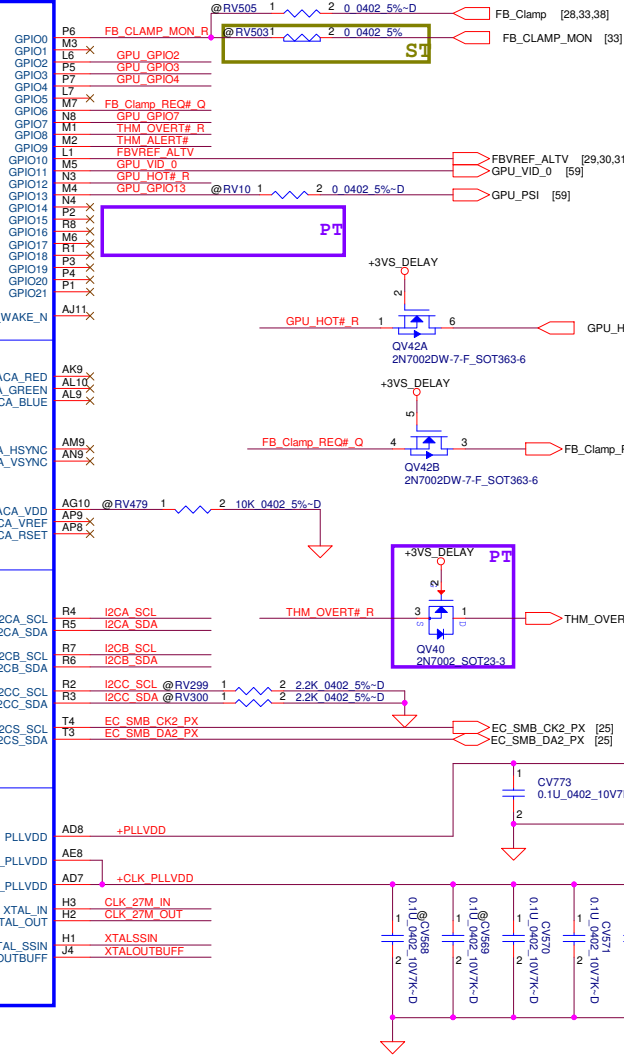
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PEG GTX C_HRX_N0	CV532	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N0
PEG GTX C_HRX_P1	CV533	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P1
PEG GTX C_HRX_N1	CV534	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N1
PEG GTX C_HRX_P2	CV535	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P2
PEG GTX C_HRX_N2	CV536	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N2
PEG GTX C_HRX_P3	CV537	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P3
PEG GTX C_HRX_N3	CV538	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N3
PEG GTX C_HRX_P4	CV539	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P4
PEG GTX C_HRX_N4	CV540	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N4
PEG GTX C_HRX_P5	CV541	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P5
PEG GTX C_HRX_N5	CV542	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N5
PEG GTX C_HRX_P6	CV543	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P6
PEG GTX C_HRX_N6	CV544	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N6
PEG GTX C_HRX_P7	CV545	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P7
PEG GTX C_HRX_N7	CV546	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N7
PEG GTX C_HRX_P8	CV547	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P8
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PEG GTX C_HRX_N9	CV551	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N9
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PEG GTX C_HRX_P12	CV560	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P12
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PEG GTX C_HRX_P14	CV564	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P14
PEG GTX C_HRX_N14	CV565	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N14
PEG GTX C_HRX_P15	CV566	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P15
PEG GTX C_HRX_N15	CV567	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N15

[17] CLK_PEG_VGA# PEX_TSTCLK_OUT#
 [17] CLK_PEG_VGA# PEX_TSTCLK_OUT#
 [18] PLTRST_VGA# PEX_TSTCLK_OUT#
 [17] PEG_A_CLKRQ# CLK_REQ#

PEG_HTX_C_GRX_P0 AN12
 PEG_HTX_C_GRX_N0 AN12
 PEG_HTX_C_GRX_P1 AN14
 PEG_HTX_C_GRX_N1 AN14
 PEG_HTX_C_GRX_P2 AP14
 PEG_HTX_C_GRX_N2 AP14
 PEG_HTX_C_GRX_P3 AN15
 PEG_HTX_C_GRX_N3 AN15
 PEG_HTX_C_GRX_P4 AN17
 PEG_HTX_C_GRX_N4 AN17
 PEG_HTX_C_GRX_P5 AP17
 PEG_HTX_C_GRX_N5 AP17
 PEG_HTX_C_GRX_P6 AN18
 PEG_HTX_C_GRX_N6 AN18
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 PEG_HTX_C_GRX_N7 AN20
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 PEG_HTX_C_GRX_N15 AN27

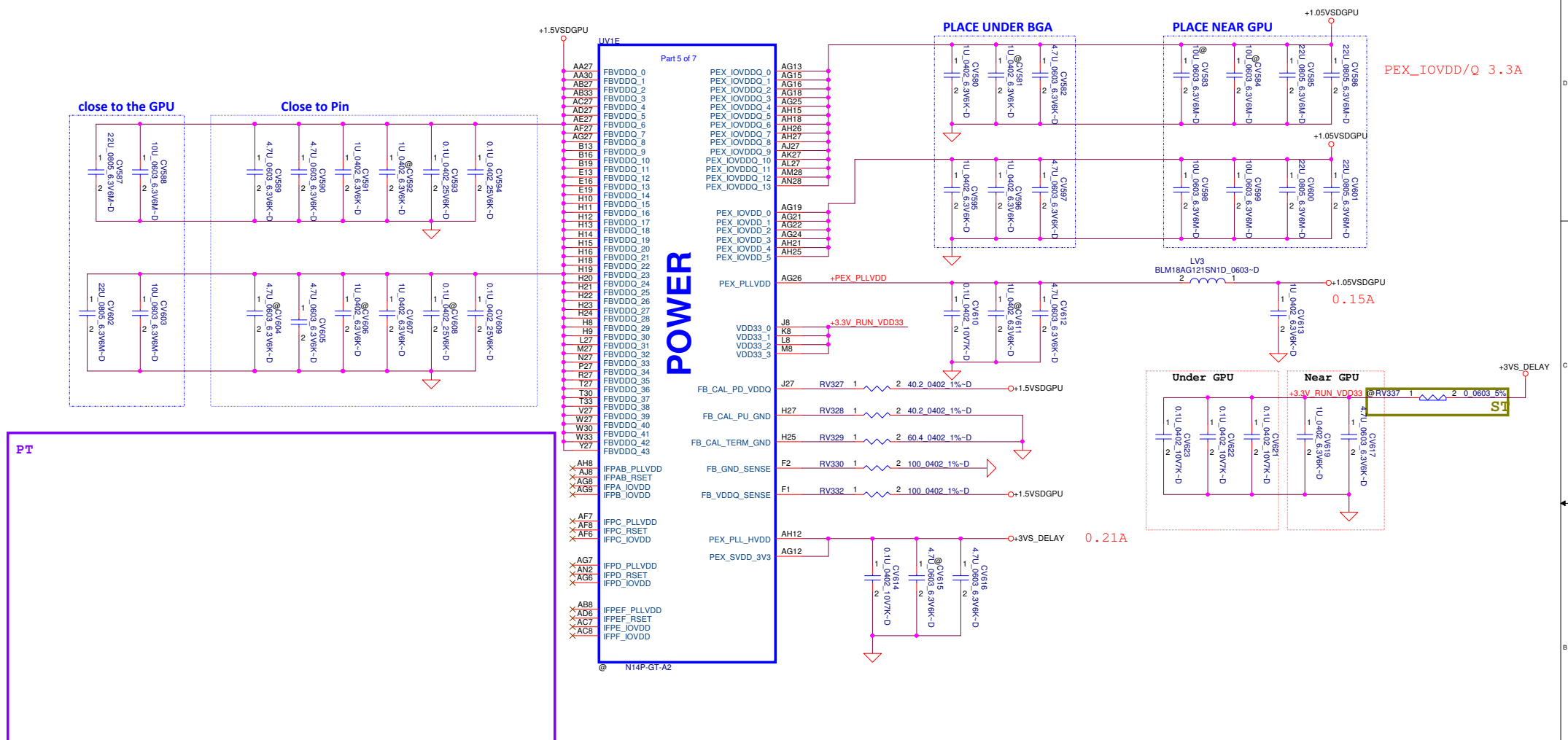
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 PEG GTX HRX_P3 AL16
 PEG GTX HRX_N3 AJ16
 PEG GTX HRX_P4 AK17
 PEG GTX HRX_N4 AJ17
 PEG GTX HRX_P5 AH17
 PEG GTX HRX_N5 AG17
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 PEG GTX HRX_P13 AH23
 PEG GTX HRX_N13 AG23
 PEG GTX HRX_P14 AK24
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 PEG GTX HRX_P15 AL25
 PEG GTX HRX_N15 AJ25

GPIO
 DACs
 PCI EXPRESS
 I2C
 CLK

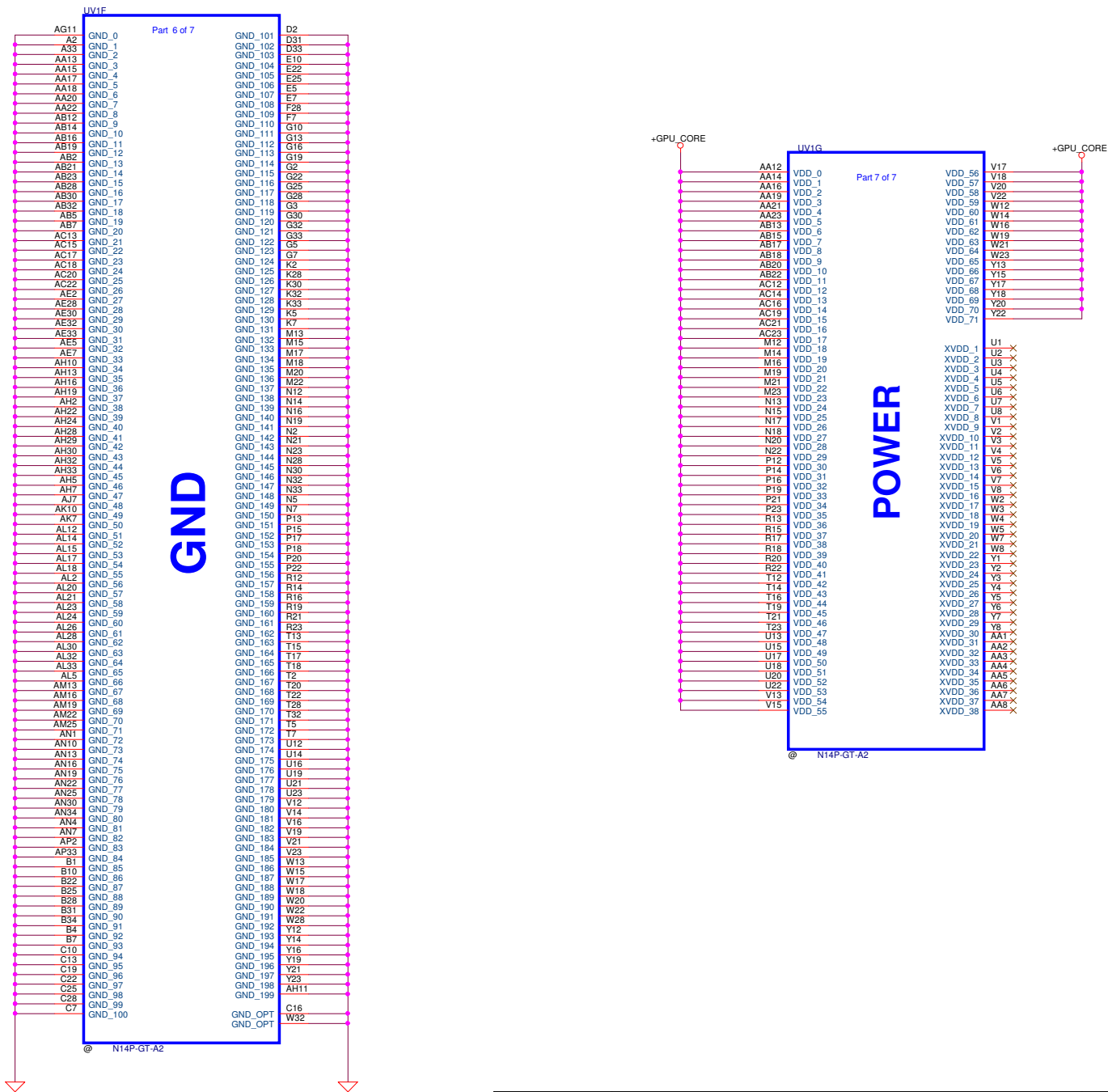


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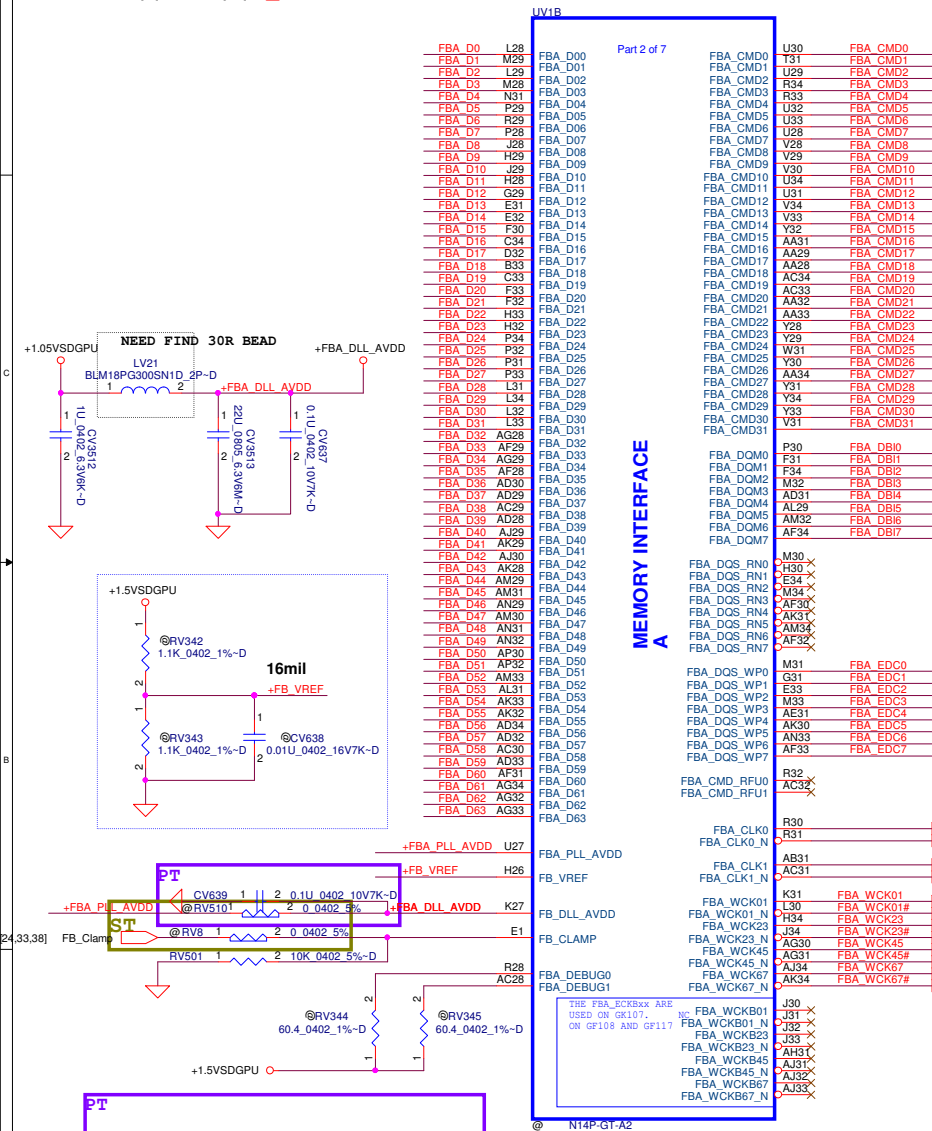
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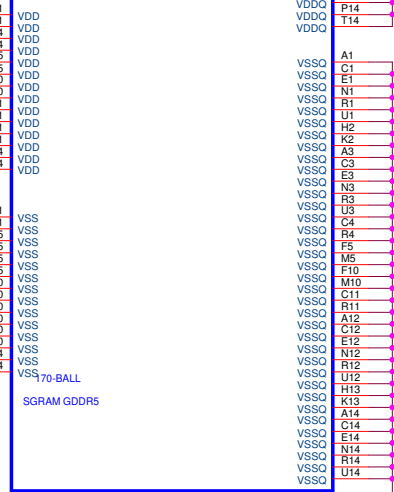
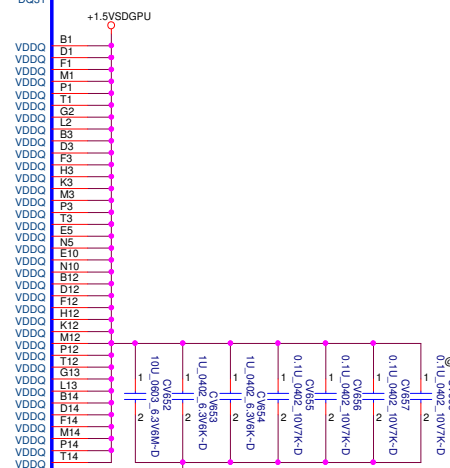
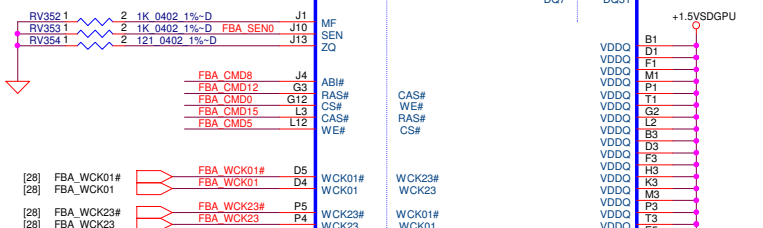
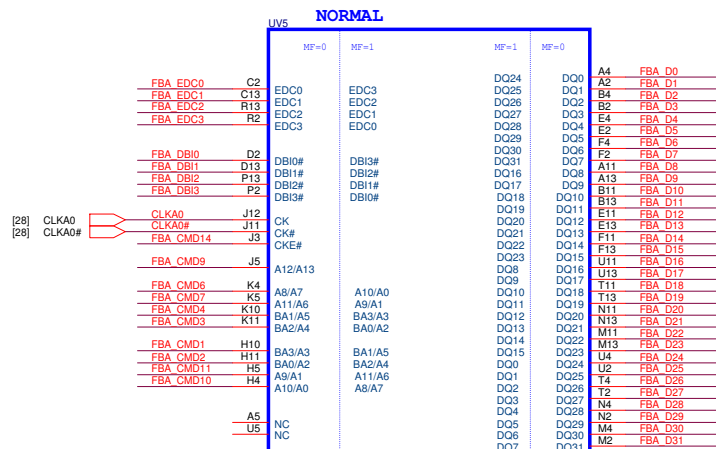
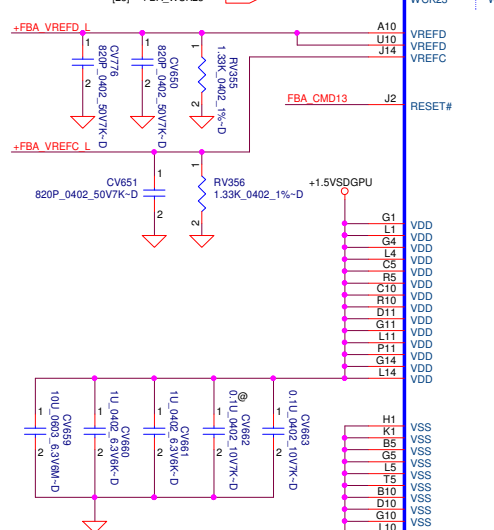
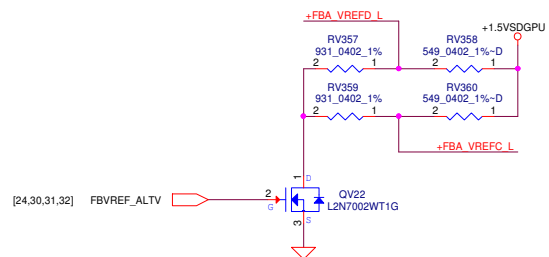
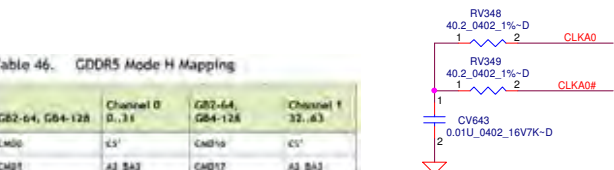
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Issued Date		2011/08/25		Deciphered Date		2012/07/25	
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				Document Number		Rev 0.1	
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[29] FBA_D[0..31] FBA_D[0..31]
 [30] FBA_D[32..63] FBA_D[32..63]
 [29..30] FBA_CMD[0..31] FBA_CMD[0..31]
 [30] FBA_DB[4..7] FBA_DB[4..7]
 [29] FBA_DB[0..3] FBA_DB[0..3]
 [30] FBA_EDC[4..7] FBA_EDC[4..7]
 [29] FBA_EDC[0..3] FBA_EDC[0..3]

[31] FBB_D[0..31] FBB_D[0..31]
 [32] FBB_D[32..63] FBB_D[32..63]
 [31..32] FBB_CMD[0..31] FBB_CMD[0..31]
 [32] FBB_DB[4..7] FBB_DB[4..7]
 [31] FBB_DB[0..3] FBB_DB[0..3]
 [32] FBB_EDC[4..7] FBB_EDC[4..7]
 [31] FBB_EDC[0..3] FBB_EDC[0..3]



GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CM00	C5'	CM09	C5'
CM01	A1_BA3	CM17	A1_BA3
CM02	A1_BA3	CM18	A1_BA3
CM03	A4_BA2	CM19	A4_BA2
CM04	A8_BA1	CM20	A8_BA1
CM05	WE'	CM21	WE'
CM06	A7_A8	CM22	A7_A8
CM07	A8_A11	CM23	A8_A11
CM08	AB'	CM24	AB'
CM09	A12_PP1	CM25	A12_PP1
CM10	A0_A10	CM26	A0_A10
CM11	A1_A8	CM27	A1_A8
CM12	BA5'	CM28	BA5'
CM13	BS1'	CM29	BS1'
CM14	CW'	CM30	CW'
CM15	CAS'	CM31	CAS'



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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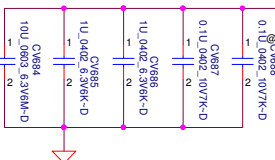
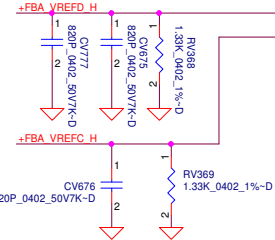
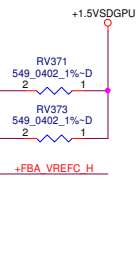
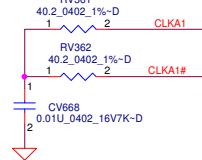
Block Diagram

Size	Document Number	Rev
		0.

Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 D _{0..31}	GB2-64, GB4-128	Channel 1 D _{32..63}
CM00	C3'	CM09	C3'
CM01	A3_BA3	CM17	A3_BA3
CM02	A3_BA5	CM18	A3_BA5
CM03	A4_BA3	CM19	A4_BA3
CM04	A8_BA1	CM20	A8_BA1
CM05	WE'	CM21	WE'
CM06	A7_A8	CM22	A7_A8
CM07	A8_A11	CM23	A8_A11
CM08	AB'	CM24	AB'
CM09	A12_PP0	CM25	A12_PP0
CM10	A0_A10	CM26	A0_A10
CM11	A1_A9	CM27	A1_A9
CM12	RAA'	CM28	RAA'
CM13	RS'	CM29	RS'
CM14	KKE'	CM30	KKE'
CM15	CA5'	CM31	CA5'



FBA_EDC4 C2
FBA_EDC5 C13
FBA_EDC6 R13
FBA_EDC7 R2

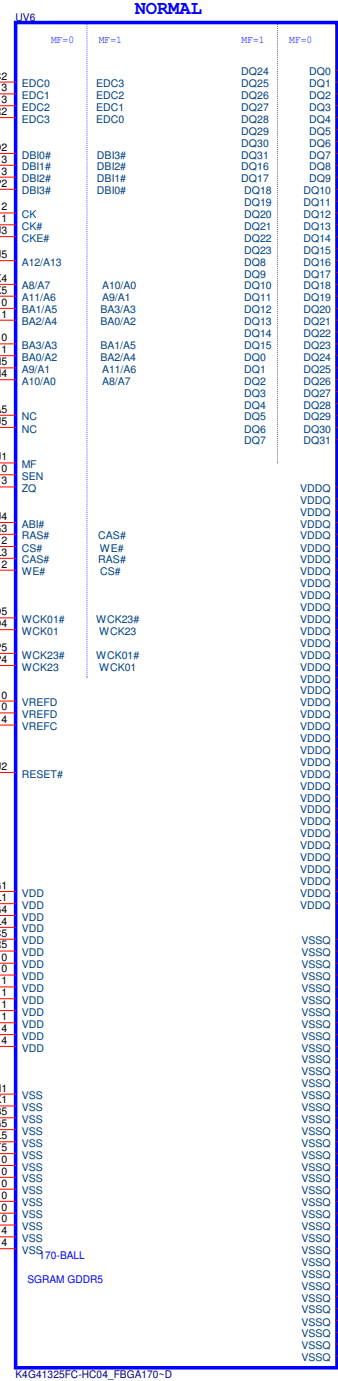
FBA_DB4 D2
FBA_DB5 D13
FBA_DB6 P13
FBA_DB7 P2

FBA_CMD25 J5
FBA_CMD22 K4
FBA_CMD23 K5
FBA_CMD20 K10
FBA_CMD19 K11

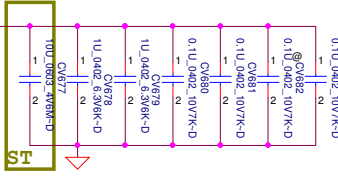
FBA_CMD17 H10
FBA_CMD18 H11
FBA_CMD27 H5
FBA_CMD26 H4

FBA_CMD24 J4
FBA_CMD28 G3
FBA_CMD16 G12
FBA_CMD31 L3
FBA_CMD21 L12

FBA_WCK45# D5
FBA_WCK45 D4
FBA_WCK67# P5
FBA_WCK67 P4



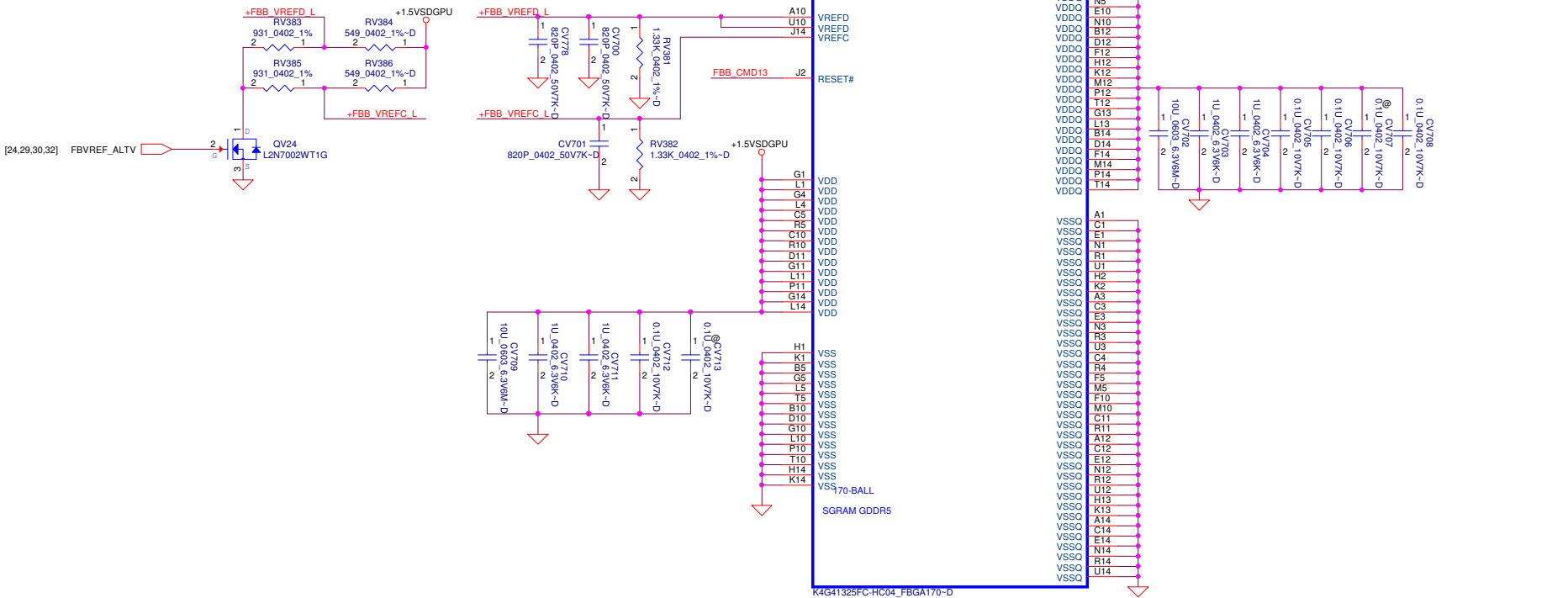
FBA_CMD[0..31] FBA_CMD[0..31] [28,29]
FBA_D[32..63] FBA_D[32..63] [28]
FBA_DB[4..7] FBA_DB[4..7] [28]
FBA_EDC[4..7] FBA_EDC[4..7] [28]



Memory Partition B - Lower 32 bits

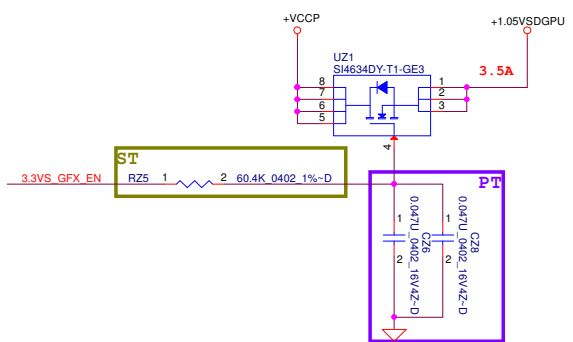
Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 D, 3.1	GB2-64, GB4-128	Channel 1 32, 63
CM00	LS ¹	CM016	CS ¹
CM01	A2, BA2	CM017	A2, BA2
CM02	A2, BA2	CM018	A2, BA2
CM03	A4, BA2	CM019	A4, BA2
CM04	A8, BA1	CM020	A8, BA1
CM05	WE ²	CM021	WE ²
CM06	A7, A8	CM022	A7, A8
CM07	A6, A11	CM023	A6, A11
CM08	AB ³	CM024	AB ³
CM09	A12, JPU	CM025	A12, JPU
CM10	A6, A10	CM026	A6, A10
CM11	A1, A9	CM027	A1, A9
CM12	BA ³	CM028	BA ³
CM13	BS ¹	CM029	BS ¹
CM14	CX ⁴	CM030	CX ⁴
CM15	CA ⁵	CM031	CA ⁵

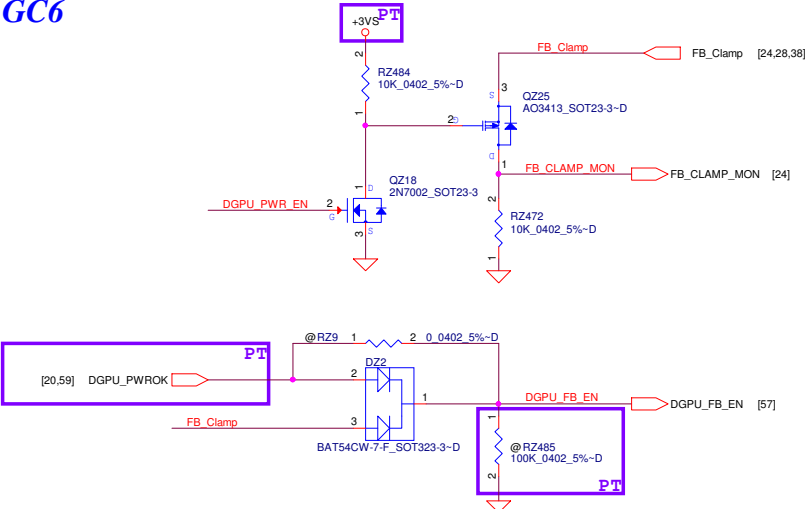


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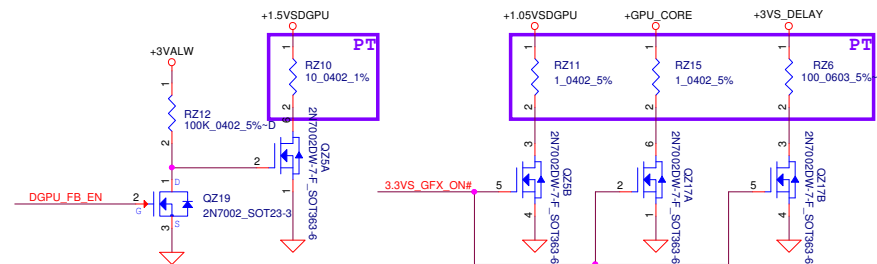
+1.05VS to +1.05VSDGPU



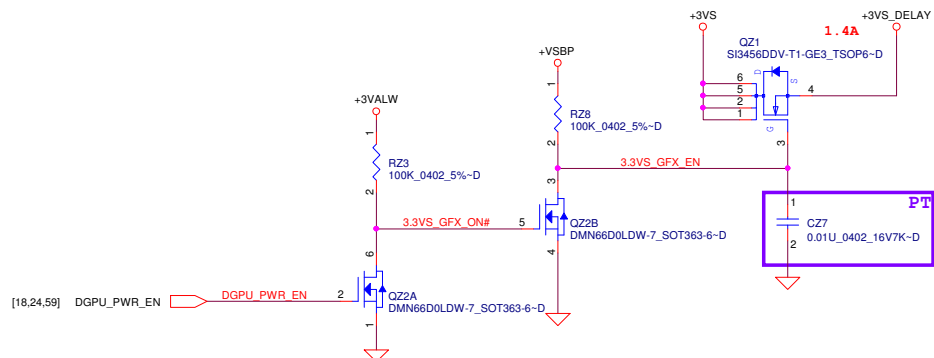
GC6



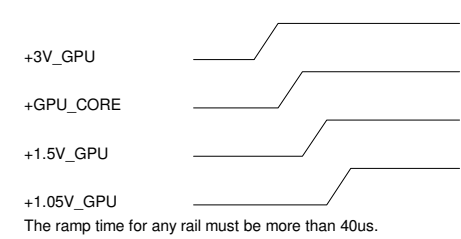
Discharge



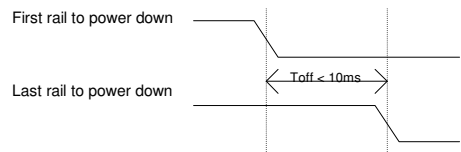
+3VS to +3VS_DELAY



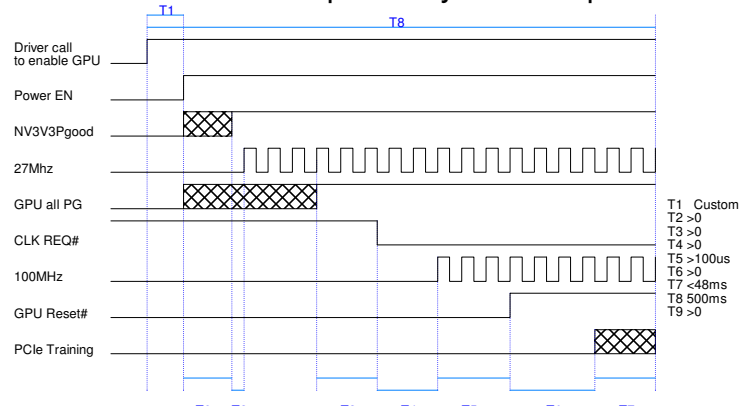
GPU Power Up Power Rail Sequence



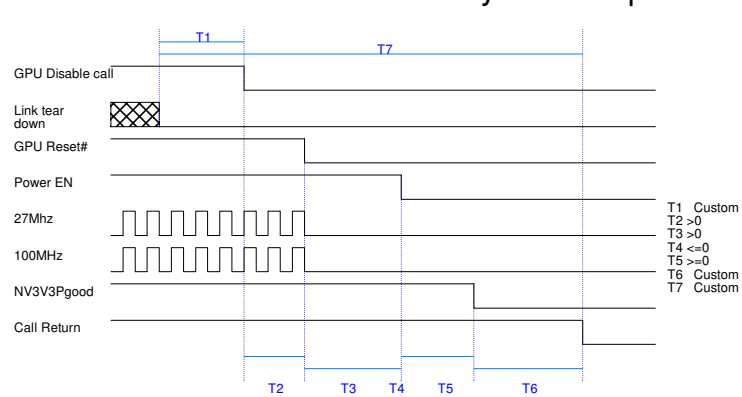
GPU Power Down Sequence



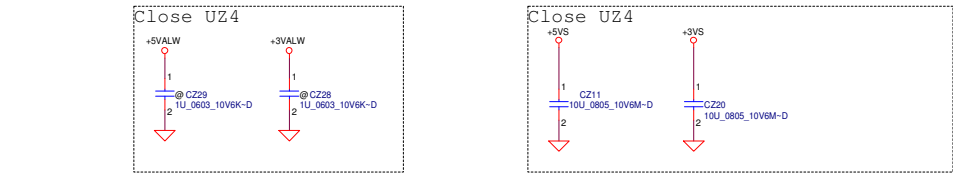
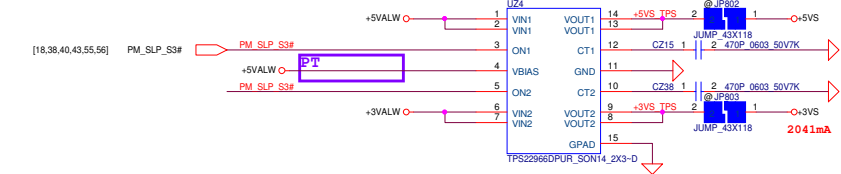
GPU Power Up Sub-system Sequence



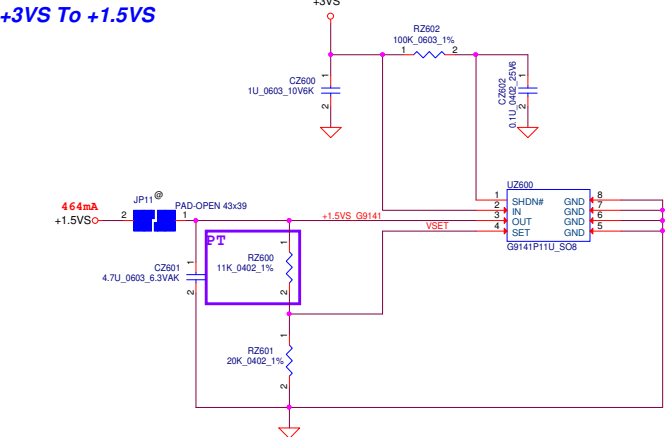
GPU Power Down Sub-system Sequence



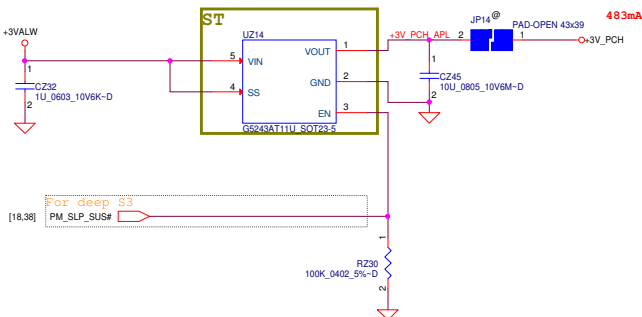
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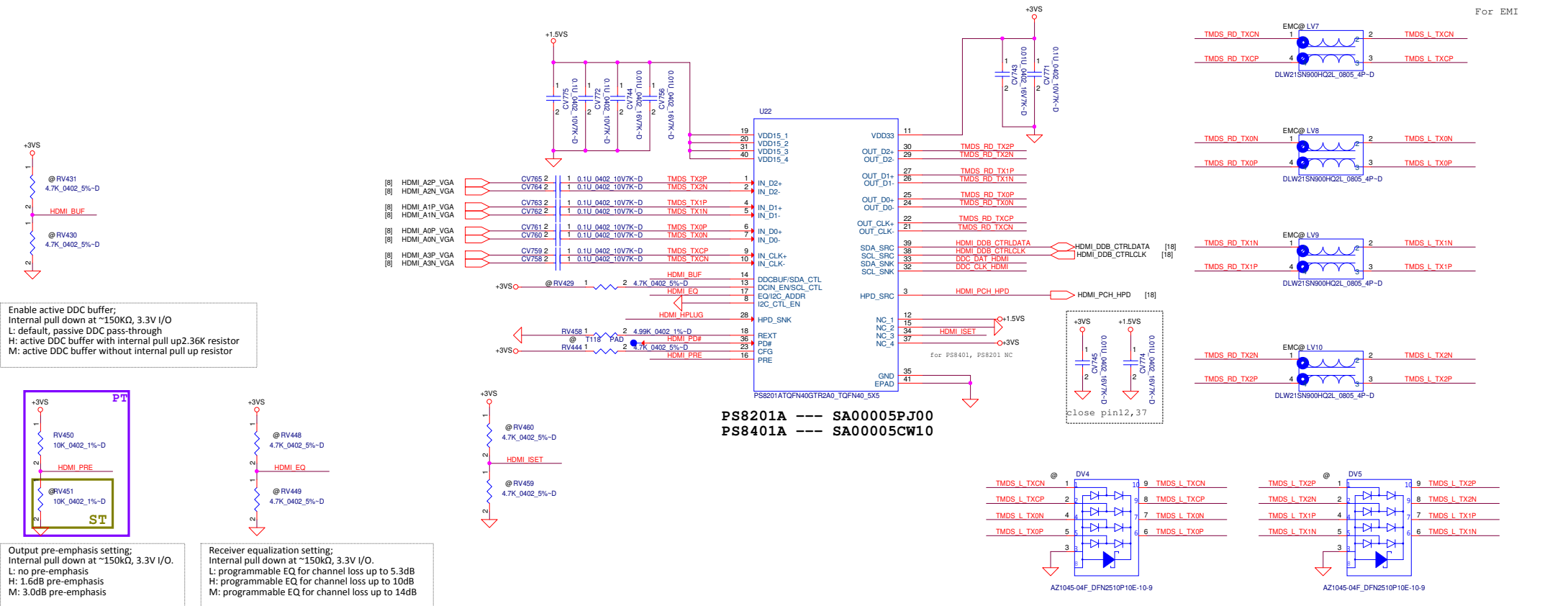
+3VS To +1.5VS



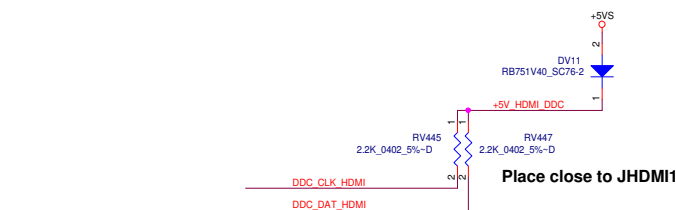
+3VALW to +3V_PCH



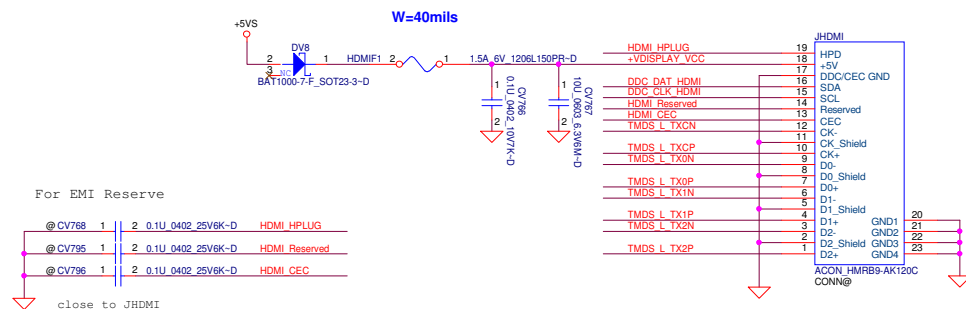
Discharge



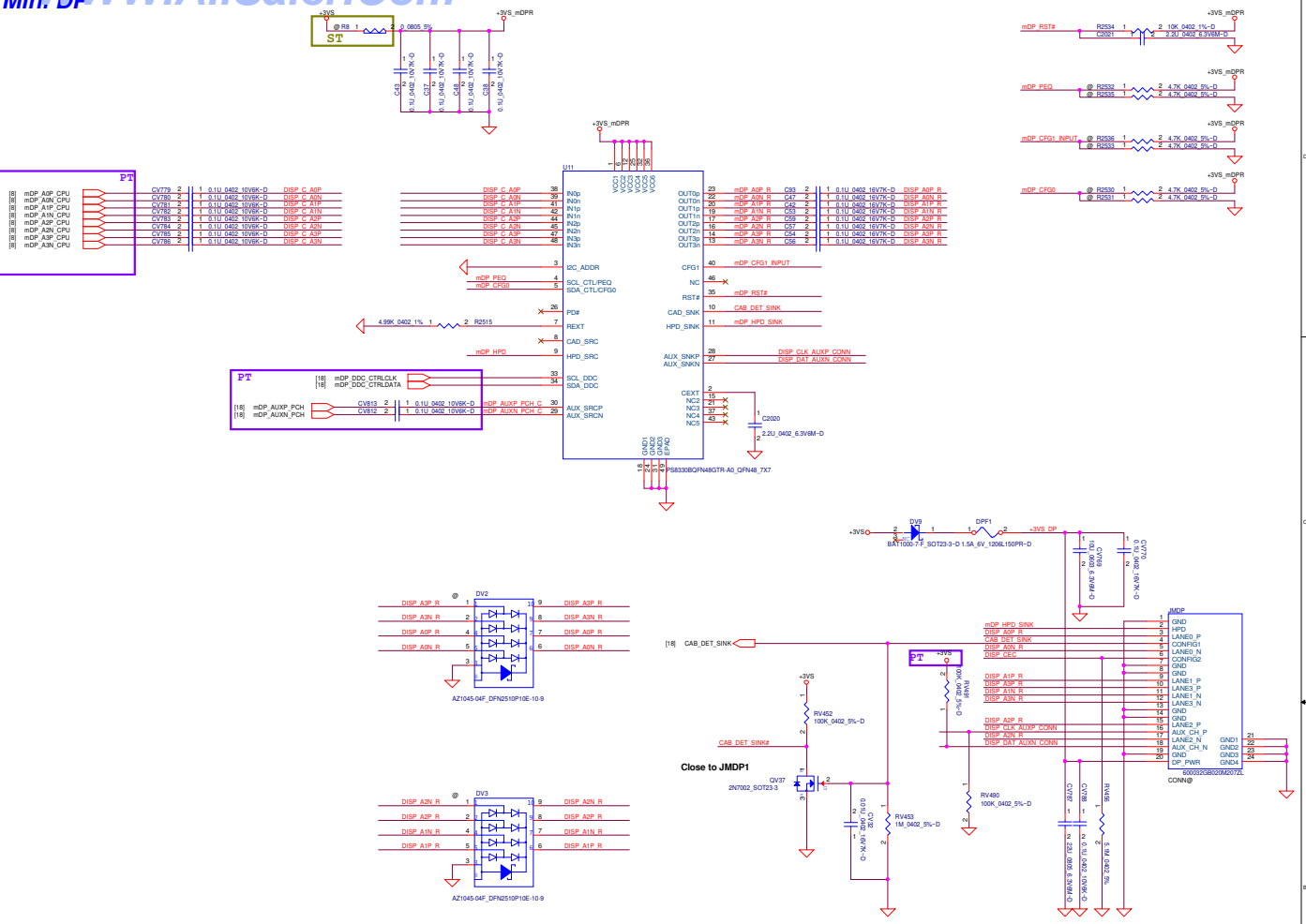
HDMI DDC



HDMI conn



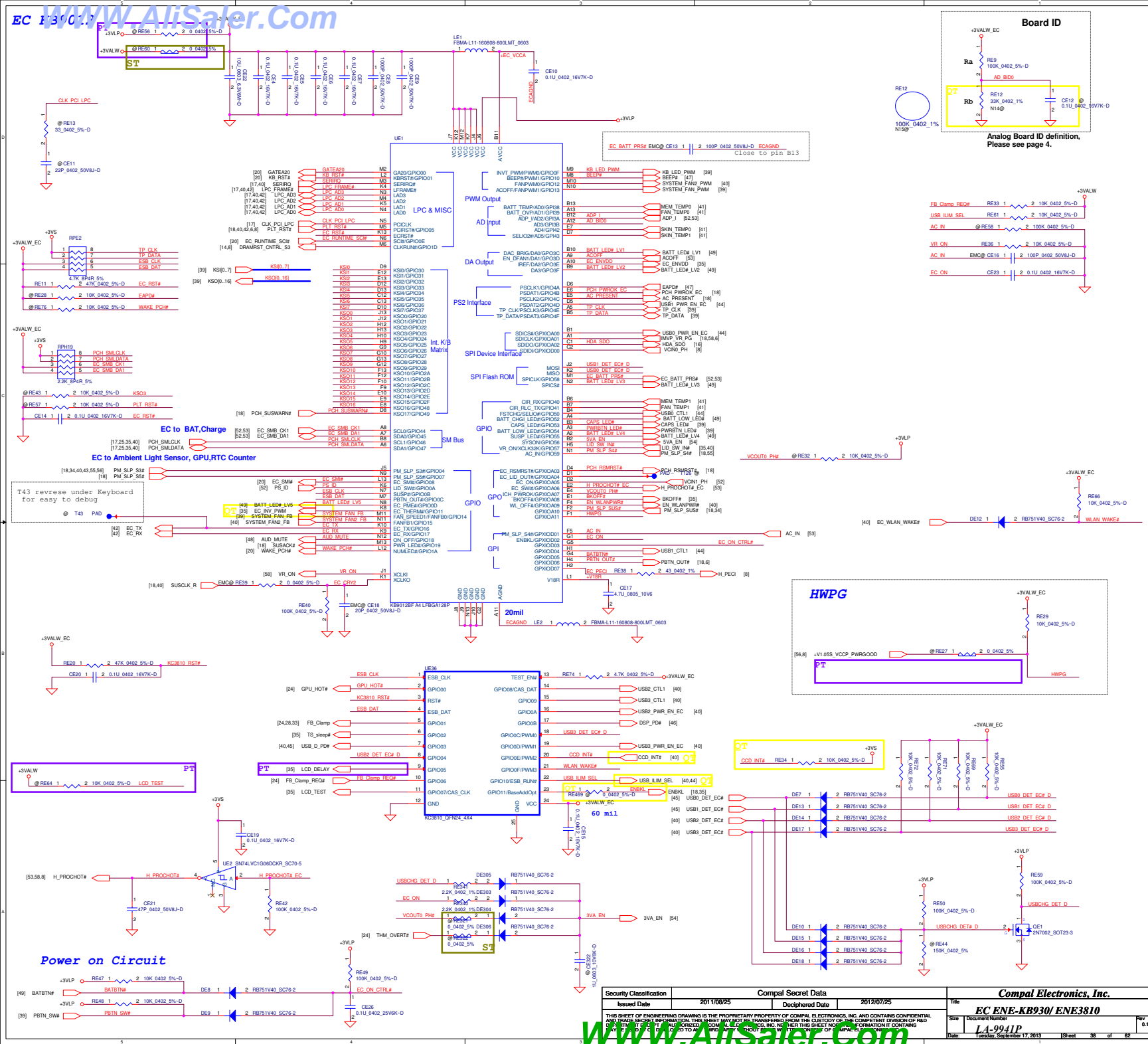
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		Custom		0.1	
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DDC Dongle SW for DP

DP HPD to PCH (iGPU)

DP HPD for DGPU output (Optimus)





PWM FAN



Touch pad



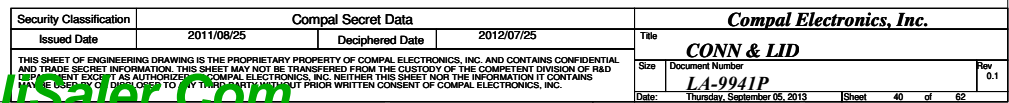
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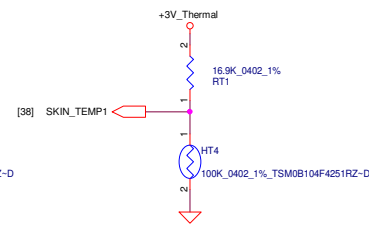
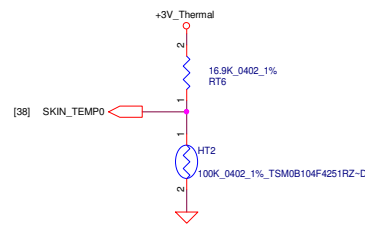
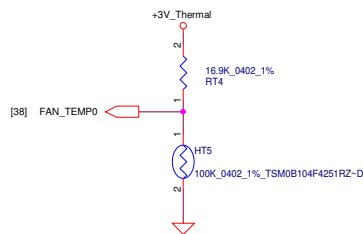
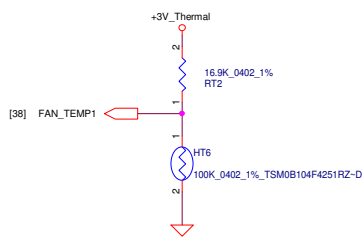
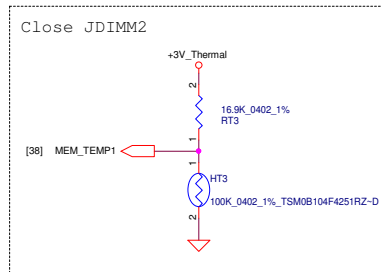
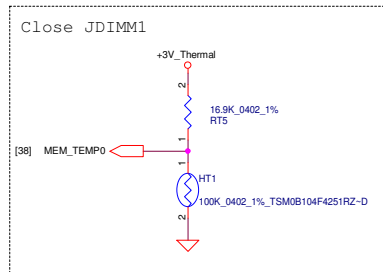
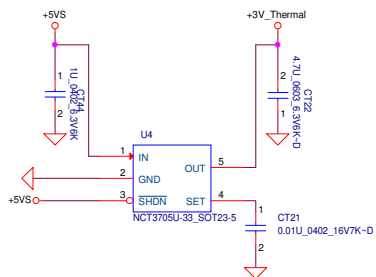


Keyboard back light



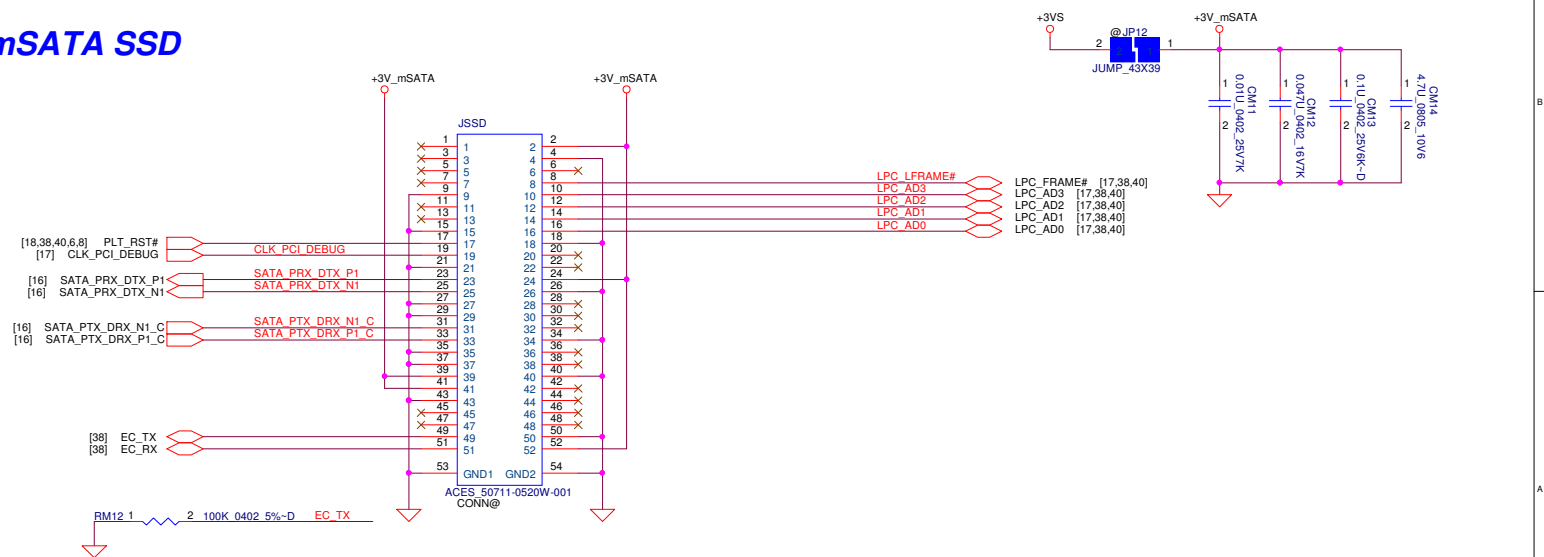
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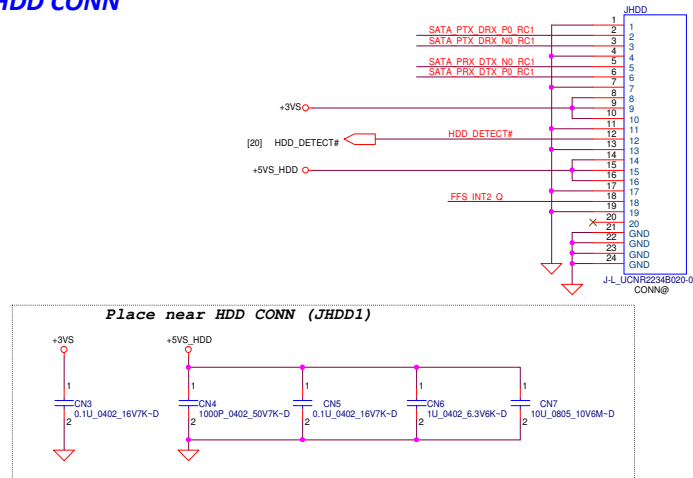


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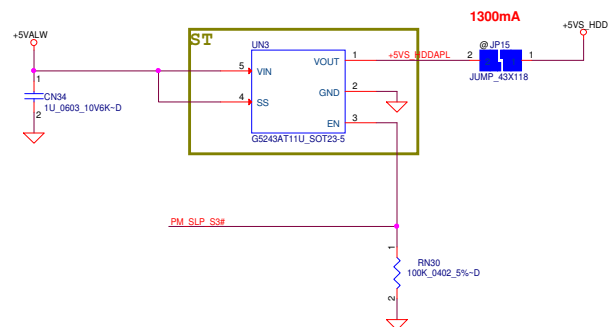
mSATA SSD



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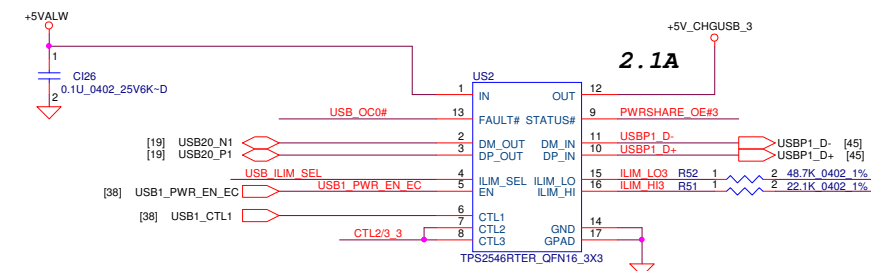
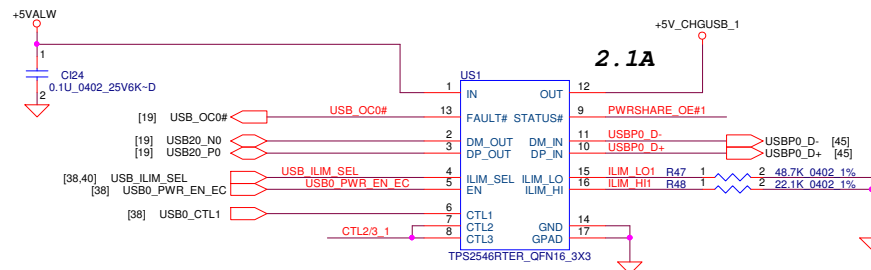
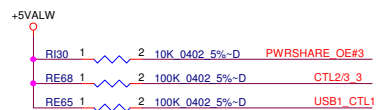
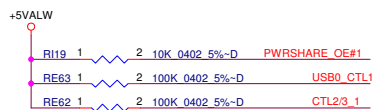


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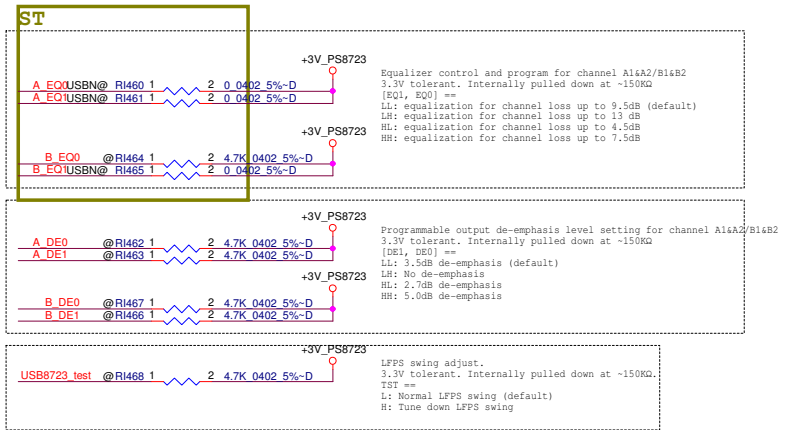
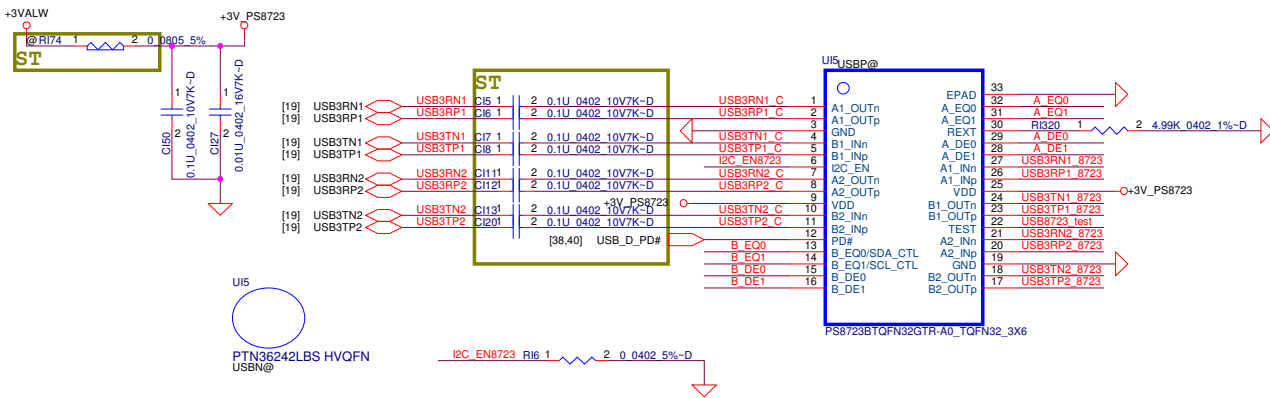


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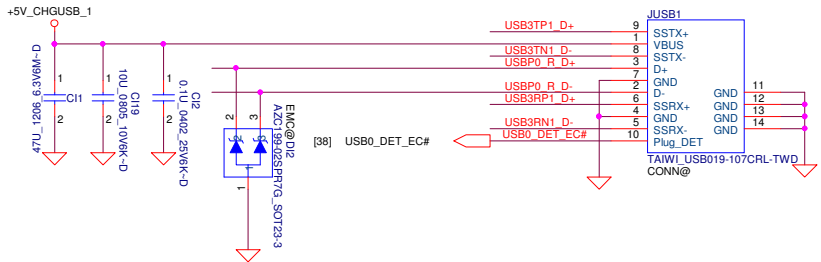
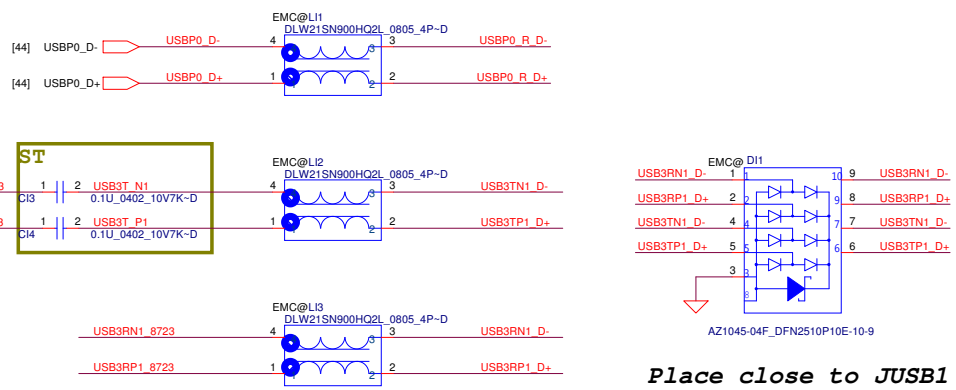
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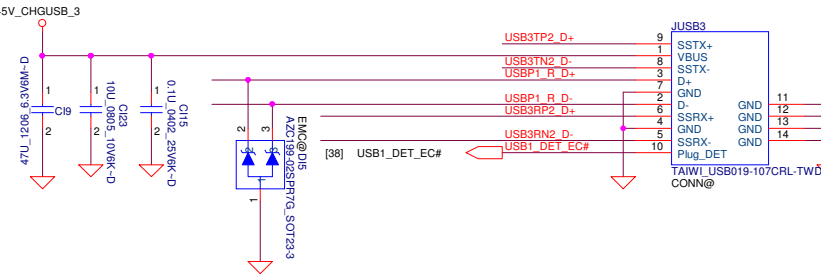
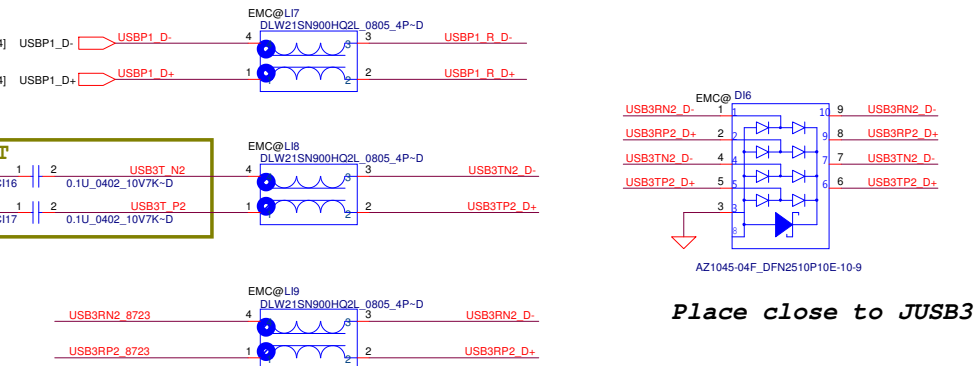
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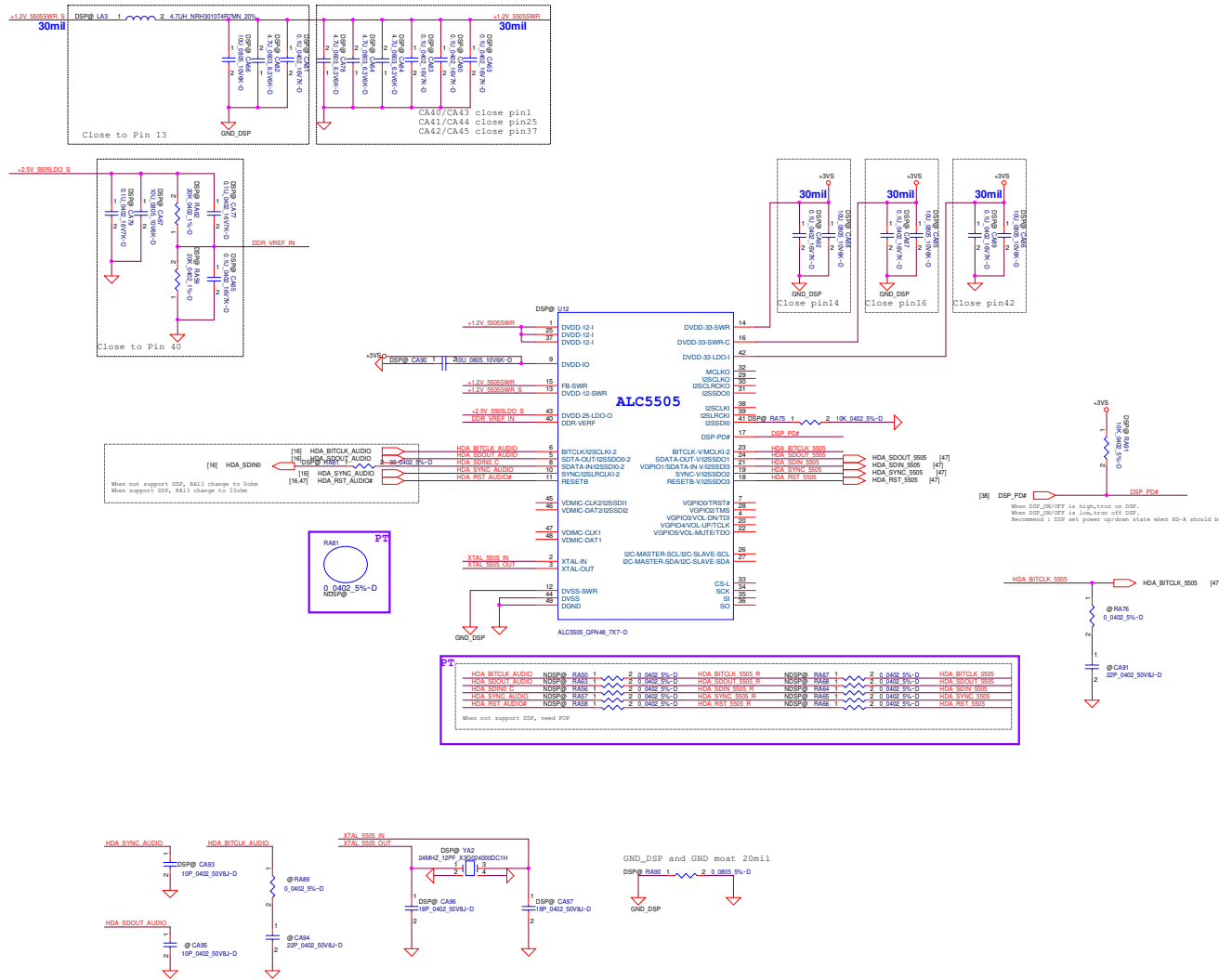
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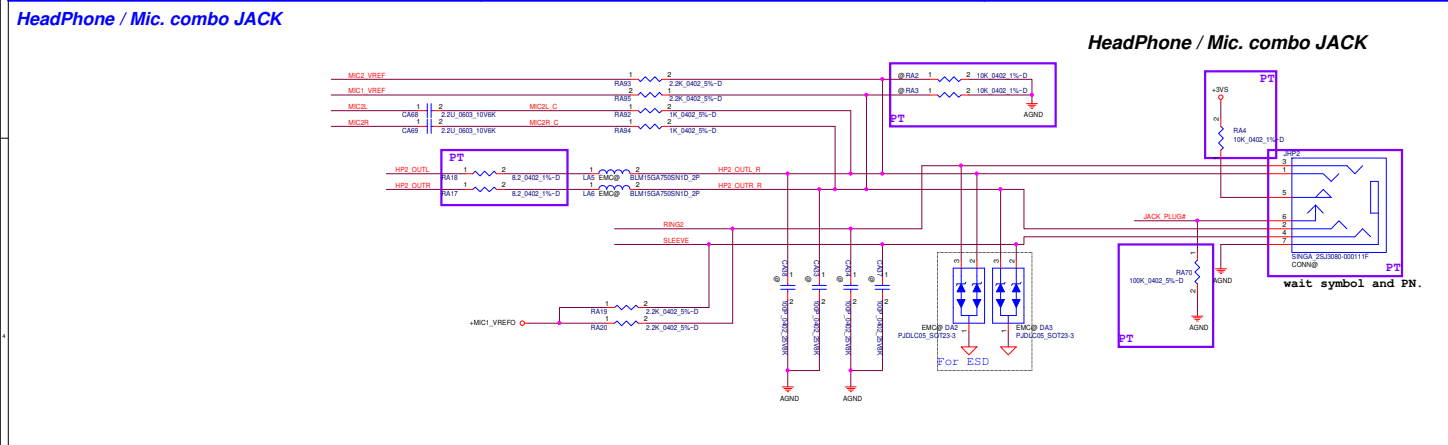
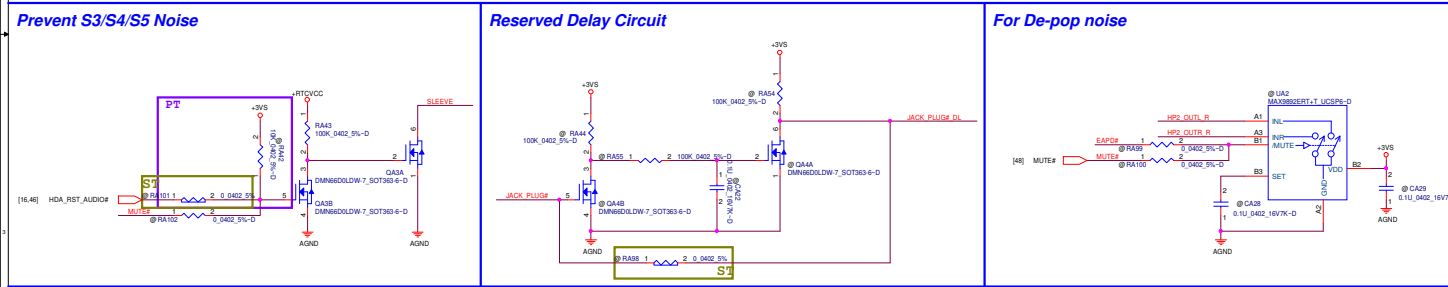
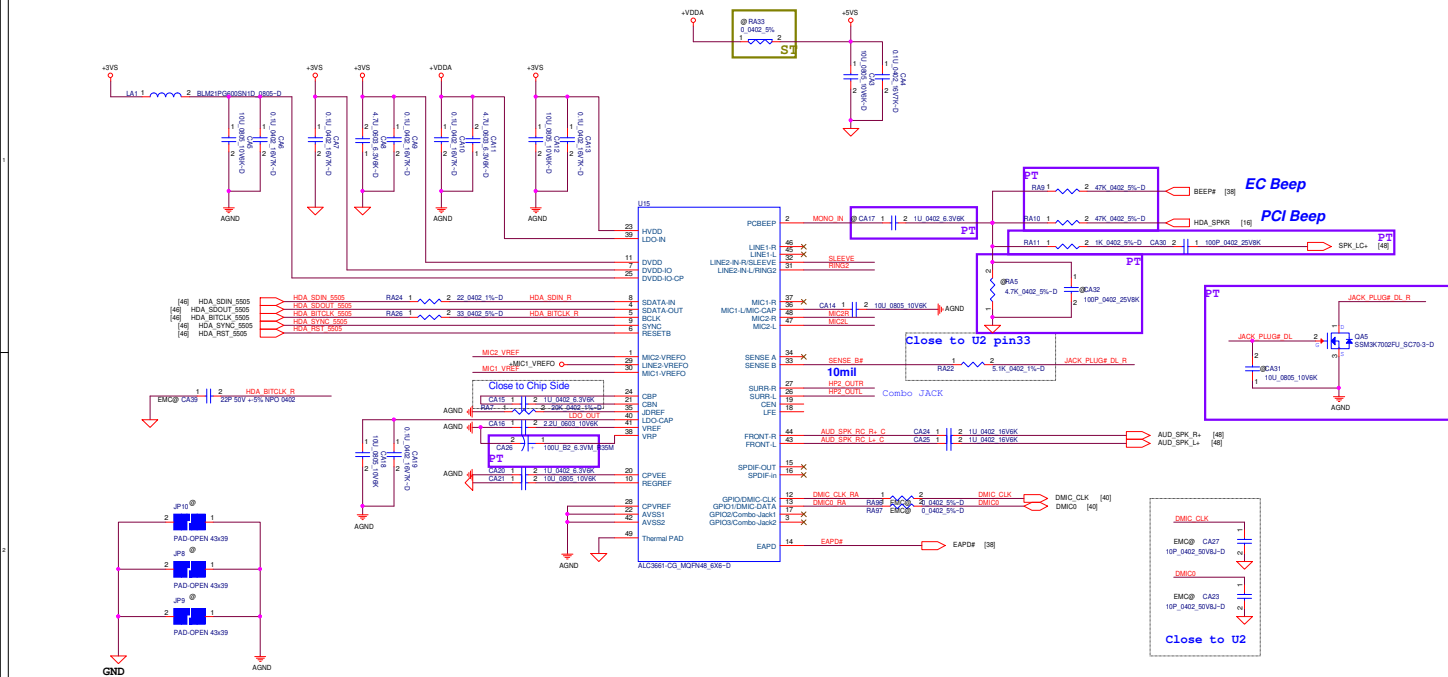
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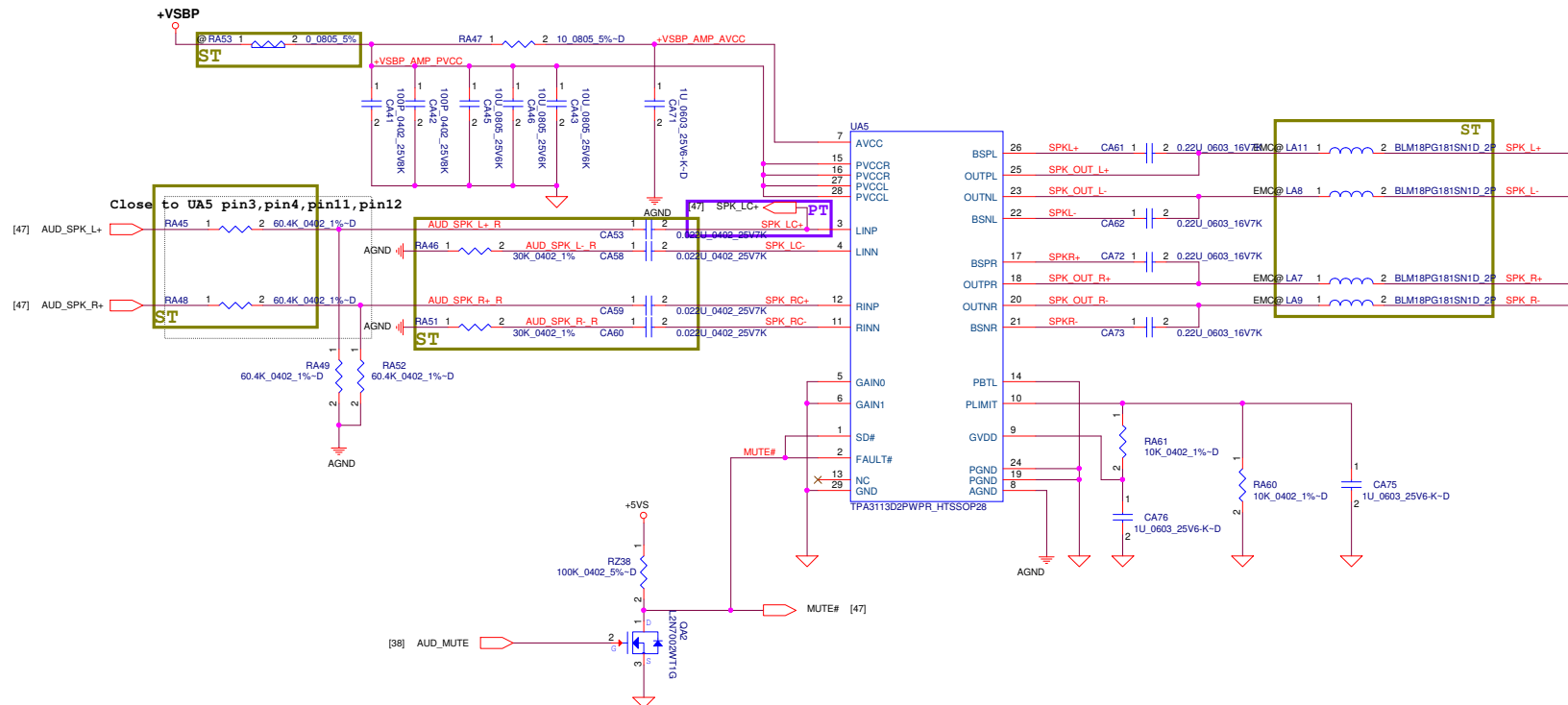


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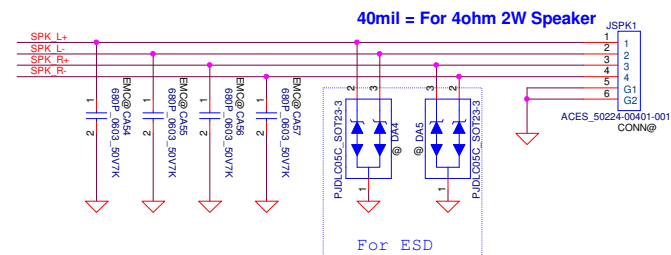


Green Clock



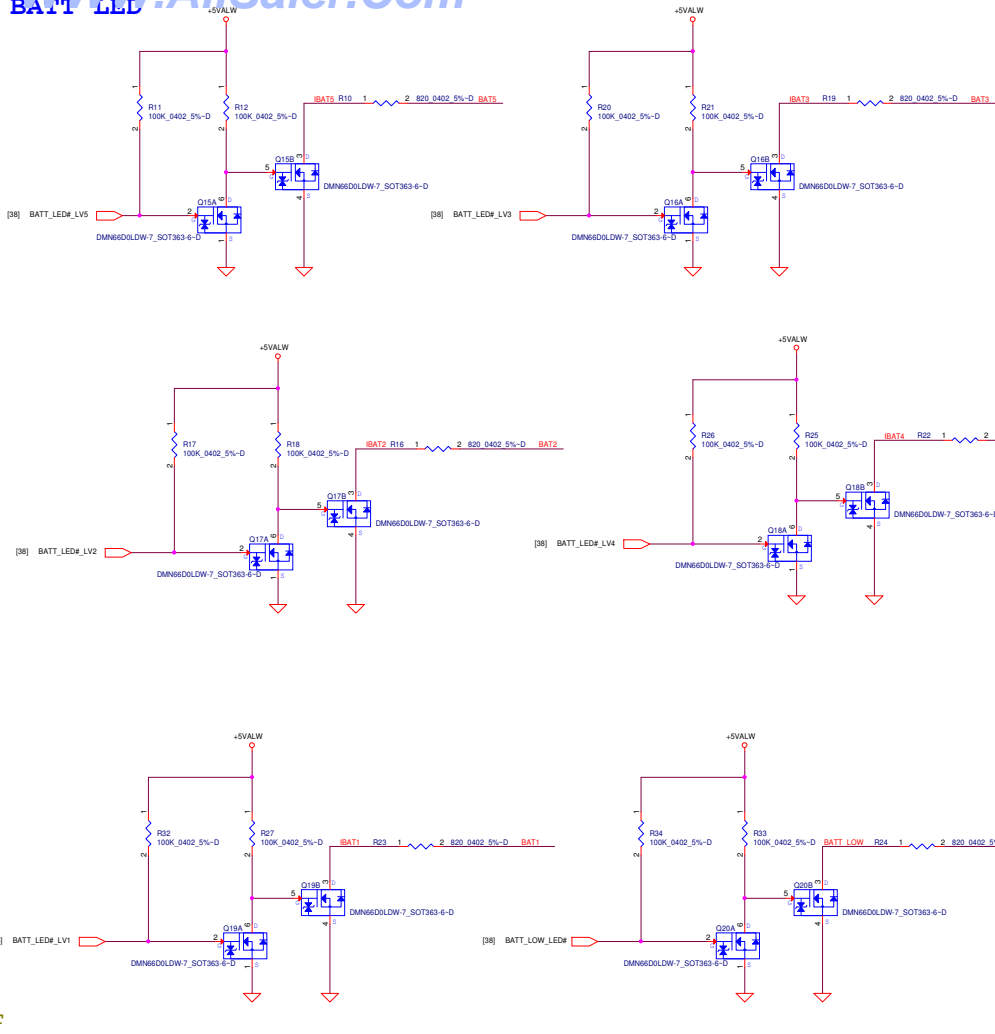


Int. Speaker Conn.

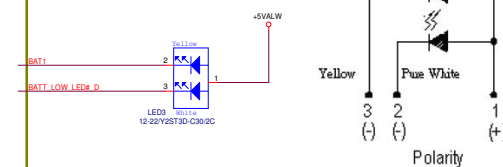
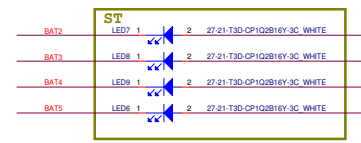
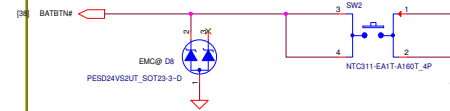


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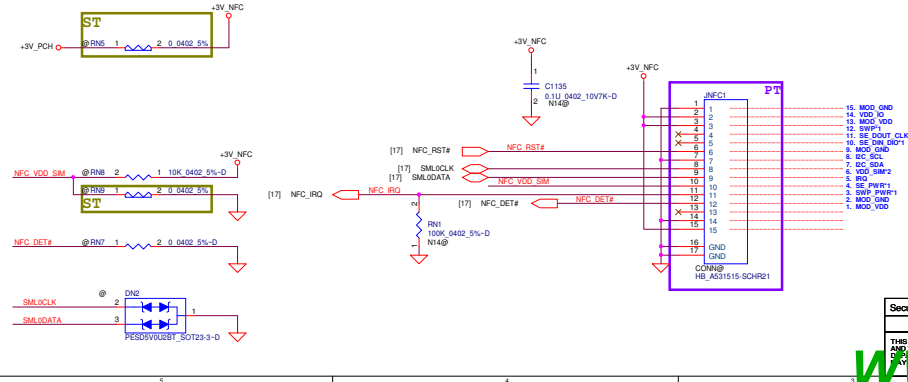
BATT_LED



BATT_LED Power Button



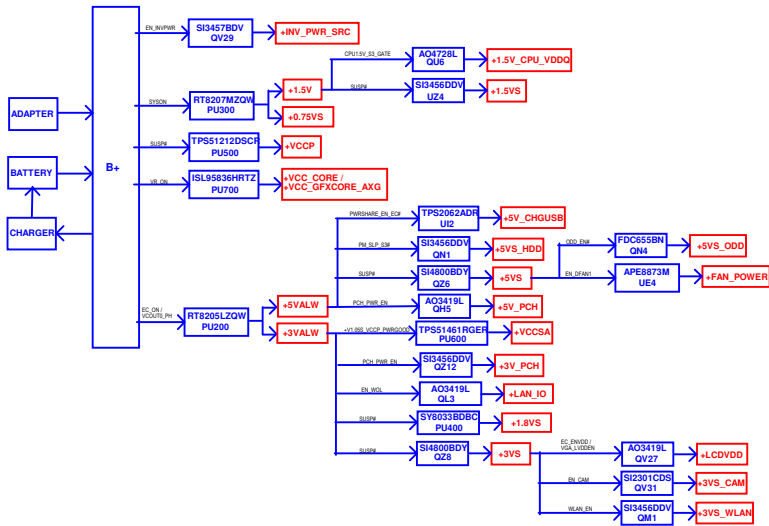
NFC Connector



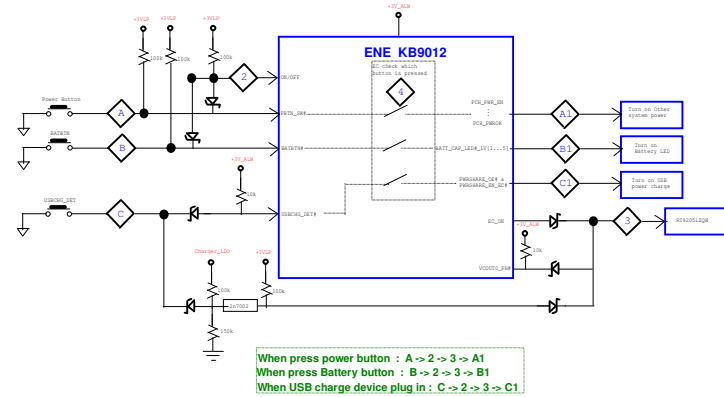
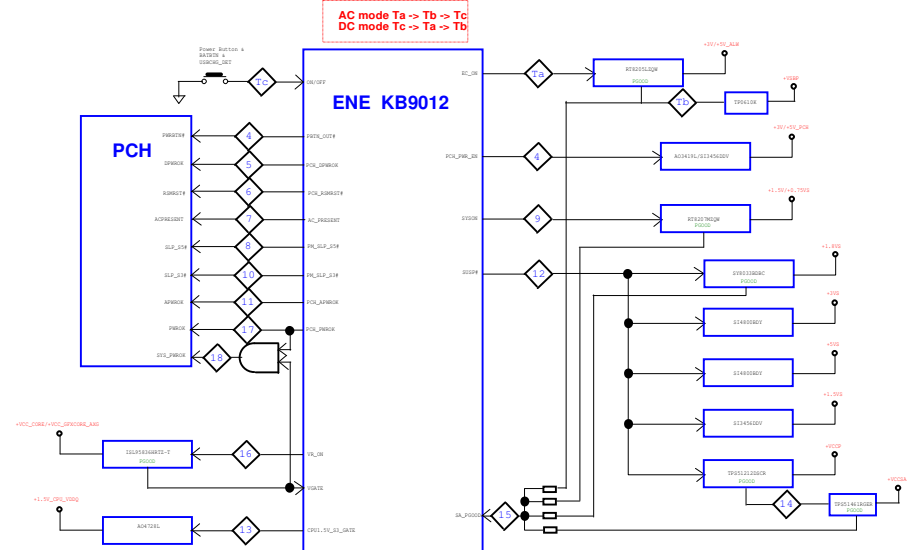
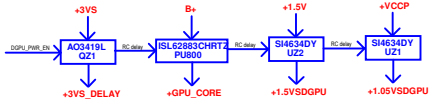
RTC counter

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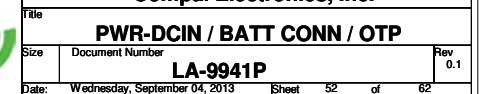
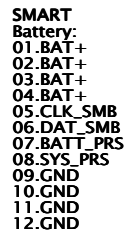
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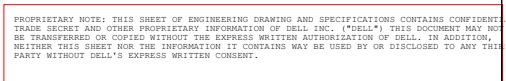


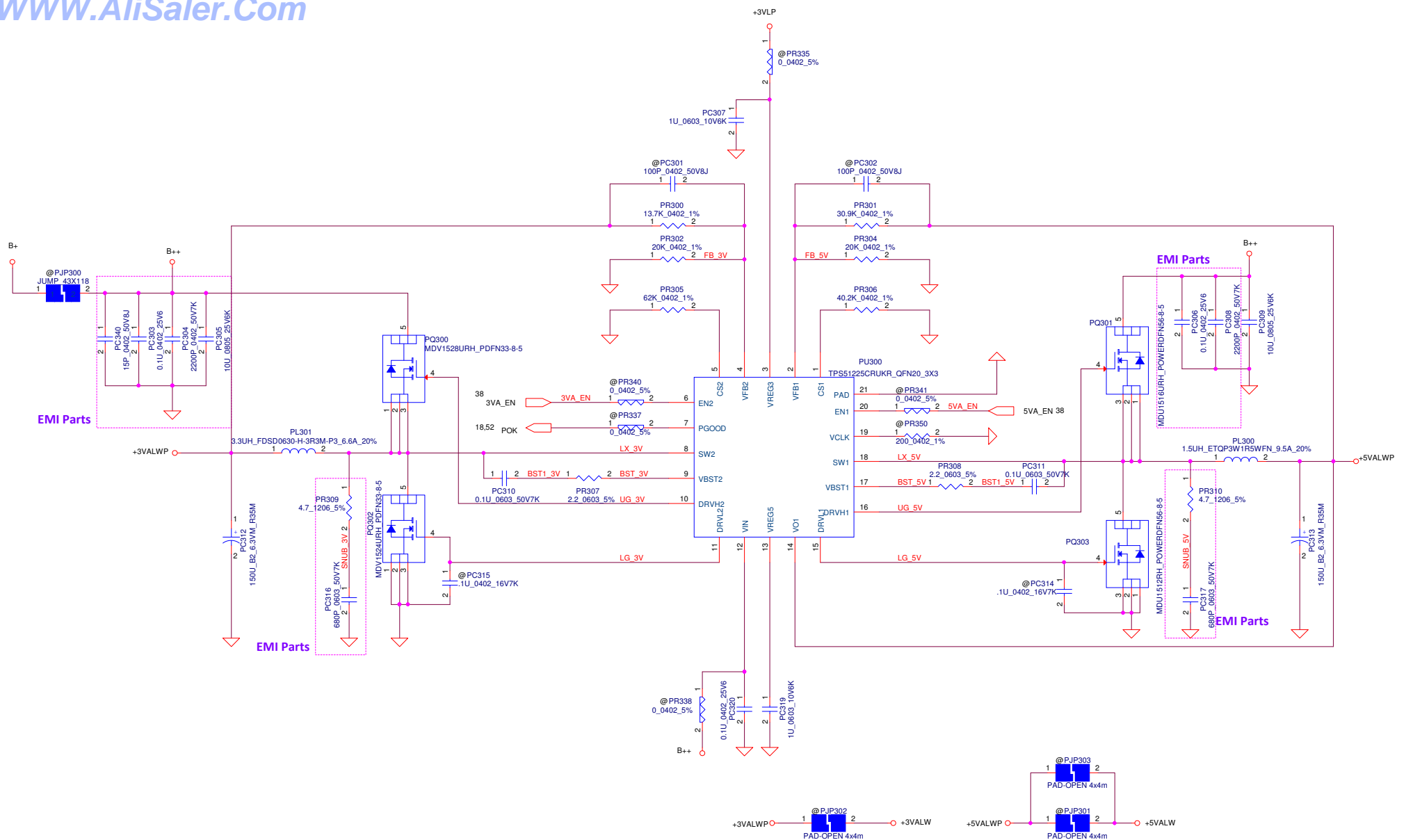
GPU



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Issued Date	2011/08/25	2012/07/25	2012/07/25	2012/07/25	2012/07/25	2012/07/25
Revised Date	2011/08/25	2012/07/25	2012/07/25	2012/07/25	2012/07/25	2012/07/25
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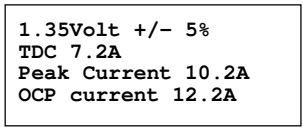
3.3VALWP
TDC 4.6A
Peak Current 6.5A
OCP current 7.8A

5VALWP
TDC 7.9A
Peak Current 11.3A
OCP current 13.4A

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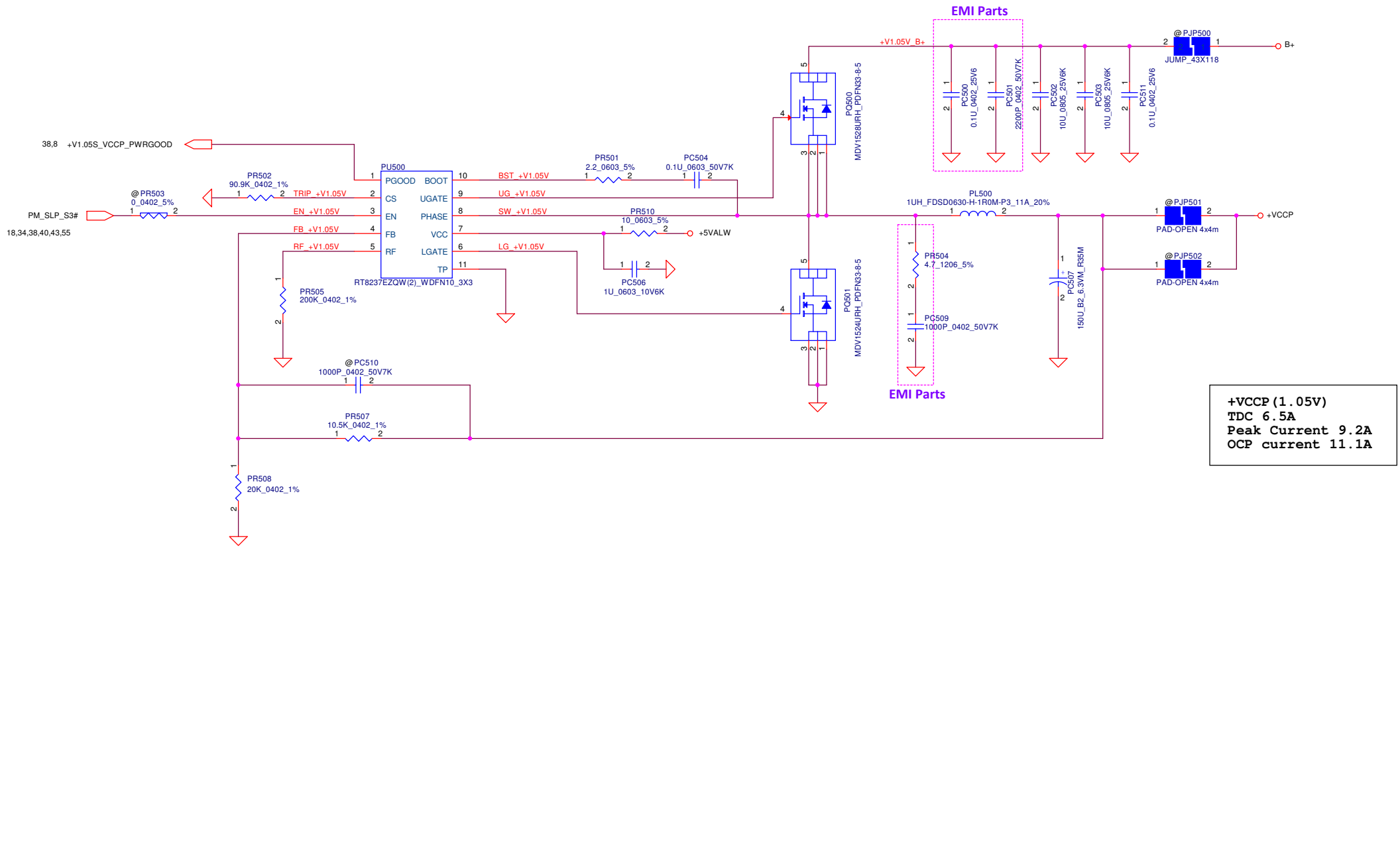


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0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.1A





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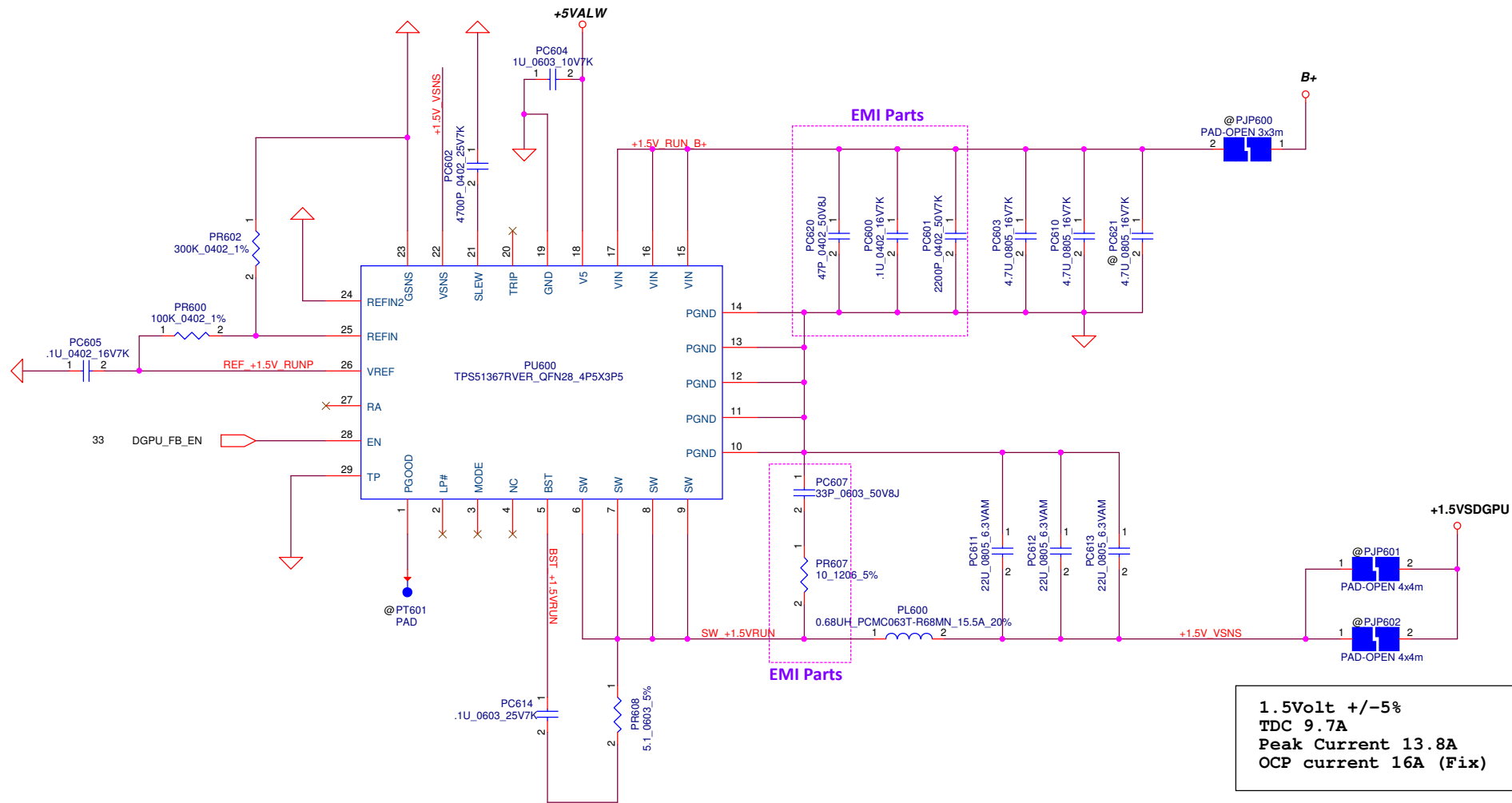


Compal Electronics, Inc.

PWR-V1.05S_VCCPP

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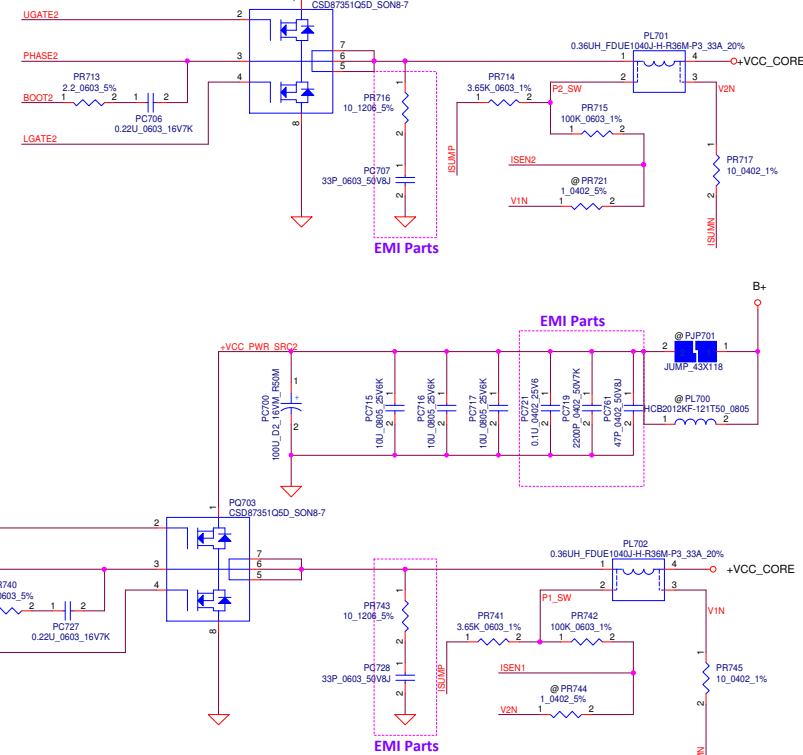


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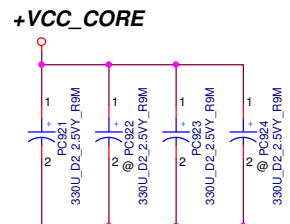
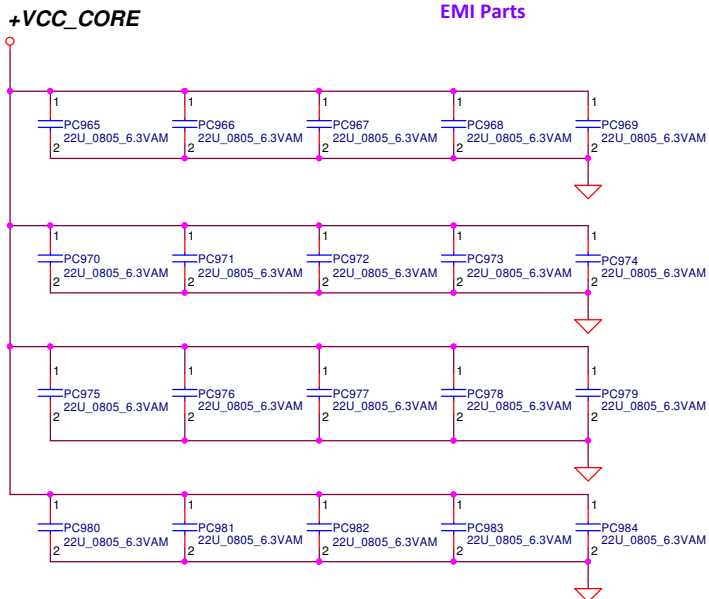
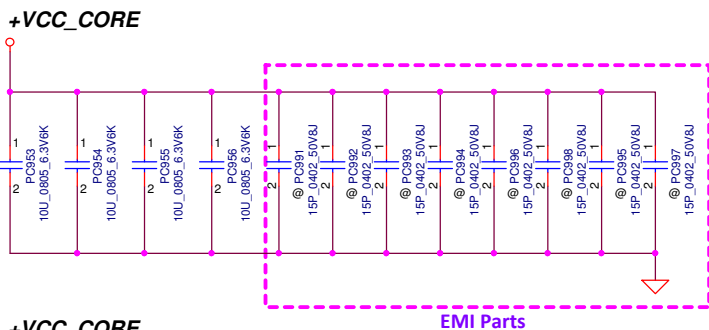
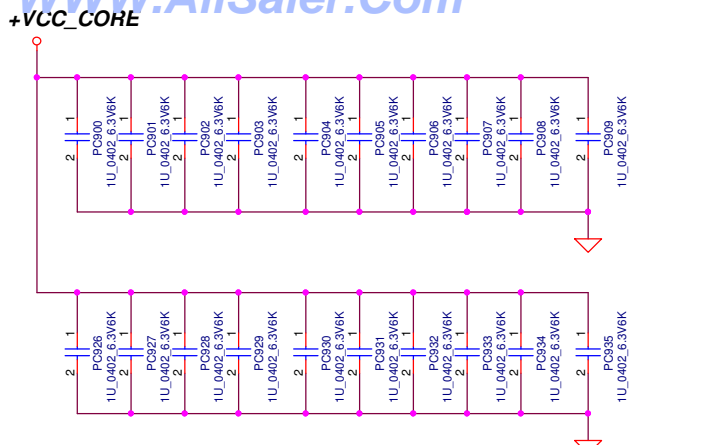


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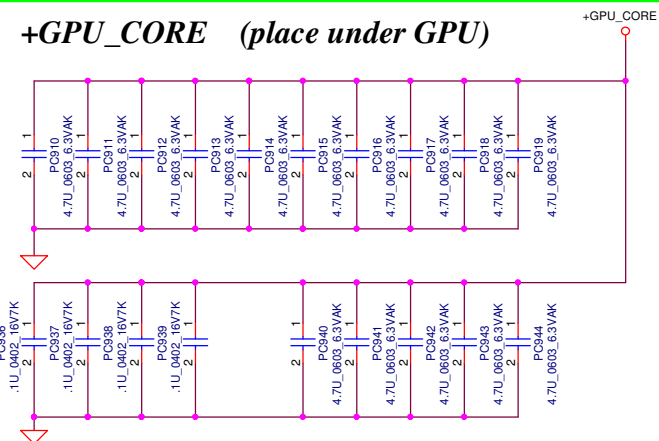




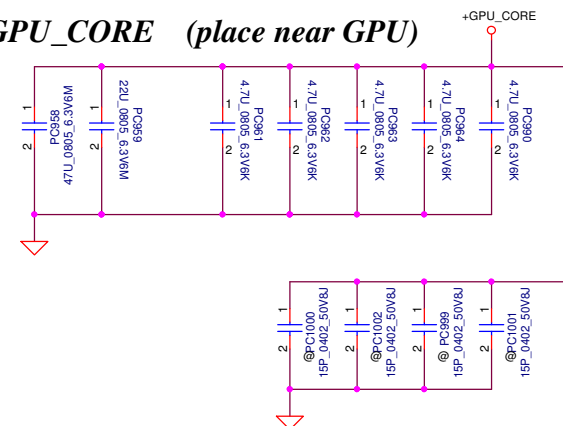
Based on PDDG
rev 1.1 Table 5-2.

Design guide:
+VCC_CORE
1. 470uF*4 (SGA0000420L)
2. 22uF*20 (SE000008L80)
3. 10uF*4 (SE160106M8L)
4. 1uF*20 (SE000000K8L)

+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



Under:
1. 4.7uF*10 (SE000008L80)
2. 0.1uF*4 (SE160106M8L)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*1 (SE000001120)
3. 47uF*1 (SE000000PL0L)
4. 33uF*1 (SGA20331E10)

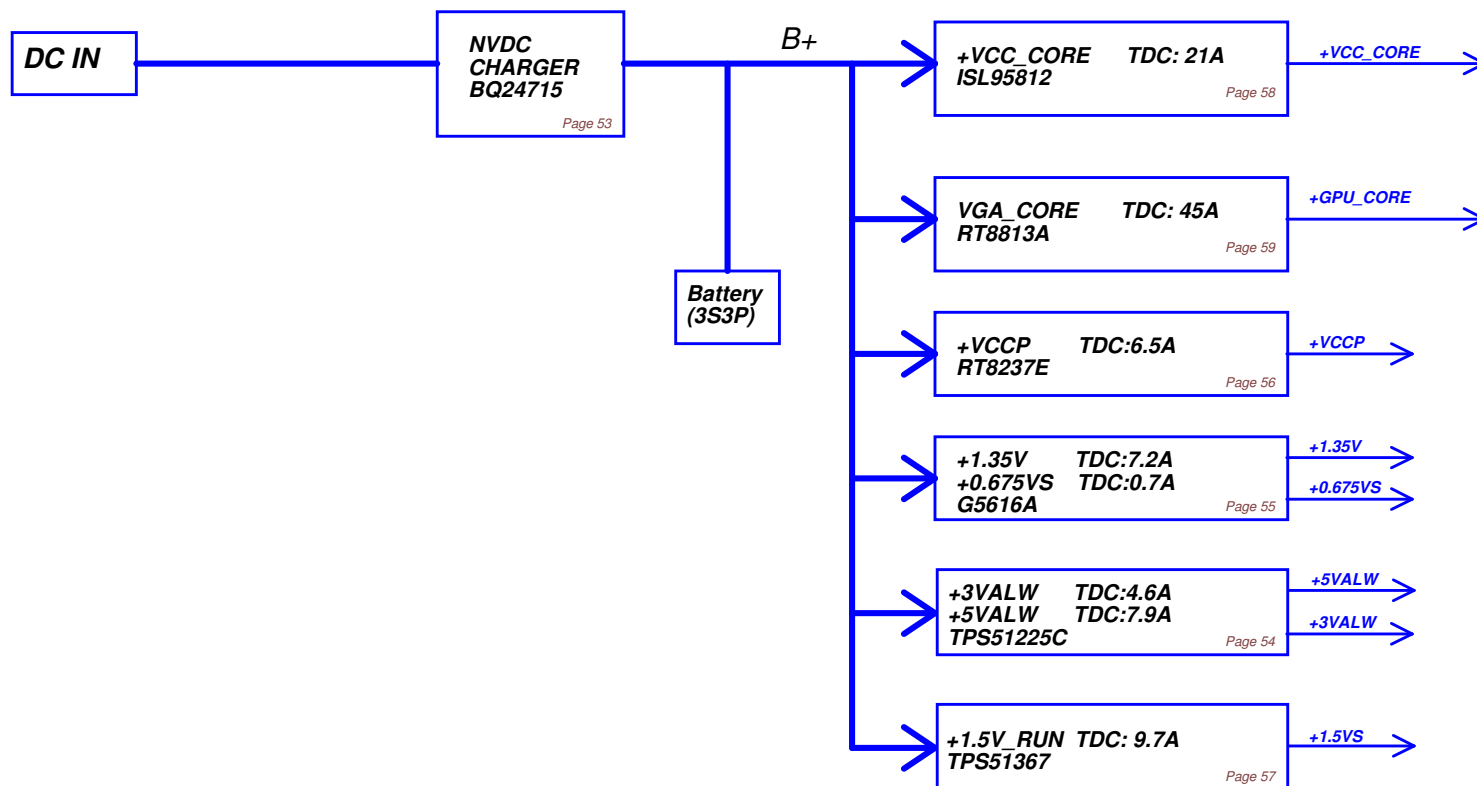
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Compal Electronics, Inc.


PROCESSOR DECOUPLING

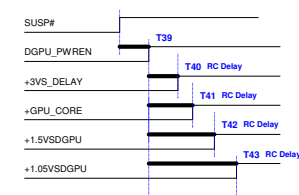
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Size Document Number
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POWER BLOCK DIAGRAM			
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